



BIOGRAPHICAL DATA

Prof. Surendra Singh Rathod



MAY 23, 2023



202-A, Plot-83, RSC-48
Gorai Shree Ganesh CHS Ltd
Opp. Pragati School
Gorai-2, Borivali (W)
Mumbai-400092



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principal.crce@fragnel.edu.in



<https://www.linkedin.com/in/dr-surendra-rathod-a1734813/>



<https://www.facebook.com/surendra.rathod.161/>



<https://www.instagram.com/ssrathod100/>



<https://twitter.com/surendr40192971>



<https://www.youtube.com/channel/UCeX4IryXvui6MRIJA6WJ98Q>

VISION

Develop myself as resourceful, helpful, skillful professionally competent teacher and always remain relevant by adopting lifelong learning attitude

SKILLS

VLSI Design and Technology, Embedded Systems, Neuromorphic Engineering, Design Thinking, Technology Law etc.

SURENDRA SINGH RATHOD

EDUCATION

- Ph.D. (Semiconductor Device and VLSI Technology), IIT Roorkee in 2011
- M.E. (Electronics), VJTI, Mumbai University in 2006.
- B.E. (Electronics and Telecom), Amaravati University in 1997

CORE VALUES

Honesty, Integrity, Hard-work, Punctuality, and Quest for excellence

LEADERSHIP

'Role Model' by demonstrating **'Leading by Example'** attitude through behavior and actions for **making a difference in life** of individuals.

PROFESSIONAL MEMBERSHIPS

IEEE Senior Member (Member 90509971)
FSAI Member (1803433): FSAI Bombay Section Student Chair
ISTE Life Member (LM-32960)
ISNT Life Member (LM-5968)

EXPERIENCE

9th Mar1998–24th Sep1999

Lecturer • F.C.R.I.T., Vashi

1st Oct 1999

Lecture • SPCE, Andheri(W), Mumbai

1st June 2007 [Approved from 19/01/2009]

Assistant Prof (5th Pay) • S.P.I.T. Andheri (West), Mumbai

3rd Aug 2008–10th June 2011

Research Scholar • Indian Institute of Technology Roorkee

16th Mar 2012 [Approved from 29th July 2013]–till date

Professor • S.P.I.T., Andheri (West), Mumbai

1st July 2022–till date

Principal • Fr. Conceicao Rodrigues College of Engg, Bandra

100+
Resource
person for
Invited Talks /
Guest
Lectures

25+
CEP/FDP/STTP
/ Workshops
attended

20+
Design
Contests and
Competitions
Organized

4 IEEE Int.
Conf. ICCICT
Organized
(Tech. Prog Chair /
Sponsorship Chair)

15+ STTP/FDP
Organized
(11 AICTE
sponsored)

Ph.D.
Completed=3
Guiding=5

Fund Received
AICTE=28.47 Lakhs
UoM=0.9Lakhs
Industry*=1.43Lakhs

Monogram=1
Book Chap.=1
Copyright=1
Mag. Articles=5

06
UDEMY
Online
Courses

***Mathworks, Quantiphi,**
Suven Consultants,
Microdevice Technologies,
SafeTTY Systems Ltd,
Barclays, J.P. Morgan, Texas
Instruments, Eduvance etc.
also contributed in Kind

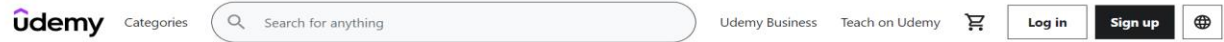
Published
Patents=08
Int. Journal=43
Int. Conf=68
Nat. Conf=26

Industry Delivered
Training Courses
Organized
Ernst and Young, Morgan
Stanley, J.P. Morgan Chase,
SAFETTY Systems Ltd., Suven
Consultants, SPJIMR etc.

Academic Engagement

Recently taught courses.....

- CMOS VLSI Design
- Analog CMOS Design
- Mixed Signal Analog Design
- HDL Programming
- ASIC Verification
- Human Health Systems Approach (HHSA)
- Law for Engineers
- Design Thinking



INSTRUCTOR **Surendra Rathod**

Professor

Total students
223

Reviews
46



My courses (6)



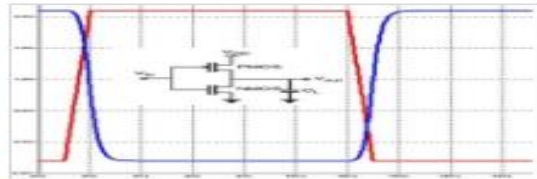
Fundamentals of Verification and System Verilog

Surendra Rathod

4.3 ★★★★★ (25)

21.5 total hours • 49 lectures • Beginner

₹1,280



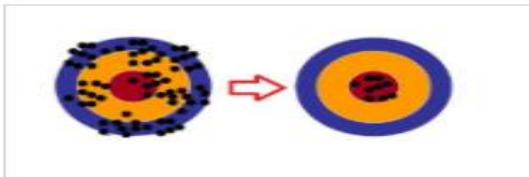
CMOS Digital VLSI Design Lab

Surendra Rathod

4.2 ★★★★★ (13)

2 total hours • 37 lectures • Beginner

₹1,280



Randomization and IPC in SystemVerilog

Surendra Rathod

4.3 ★★★★★ (3)

12.5 total hours • 47 lectures • Intermediate

₹1,280



SystemVerilog using Object Oriented Programming

Surendra Rathod

5.0 ★★★★★ (1)

8.5 total hours • 39 lectures • Intermediate

₹1,280



Functional Coverage and Assertions in SystemVerilog

Surendra Rathod

4.4 ★★★★★ (2)

8.5 total hours • 37 lectures • Intermediate

₹1,280



Technology and Indian Law

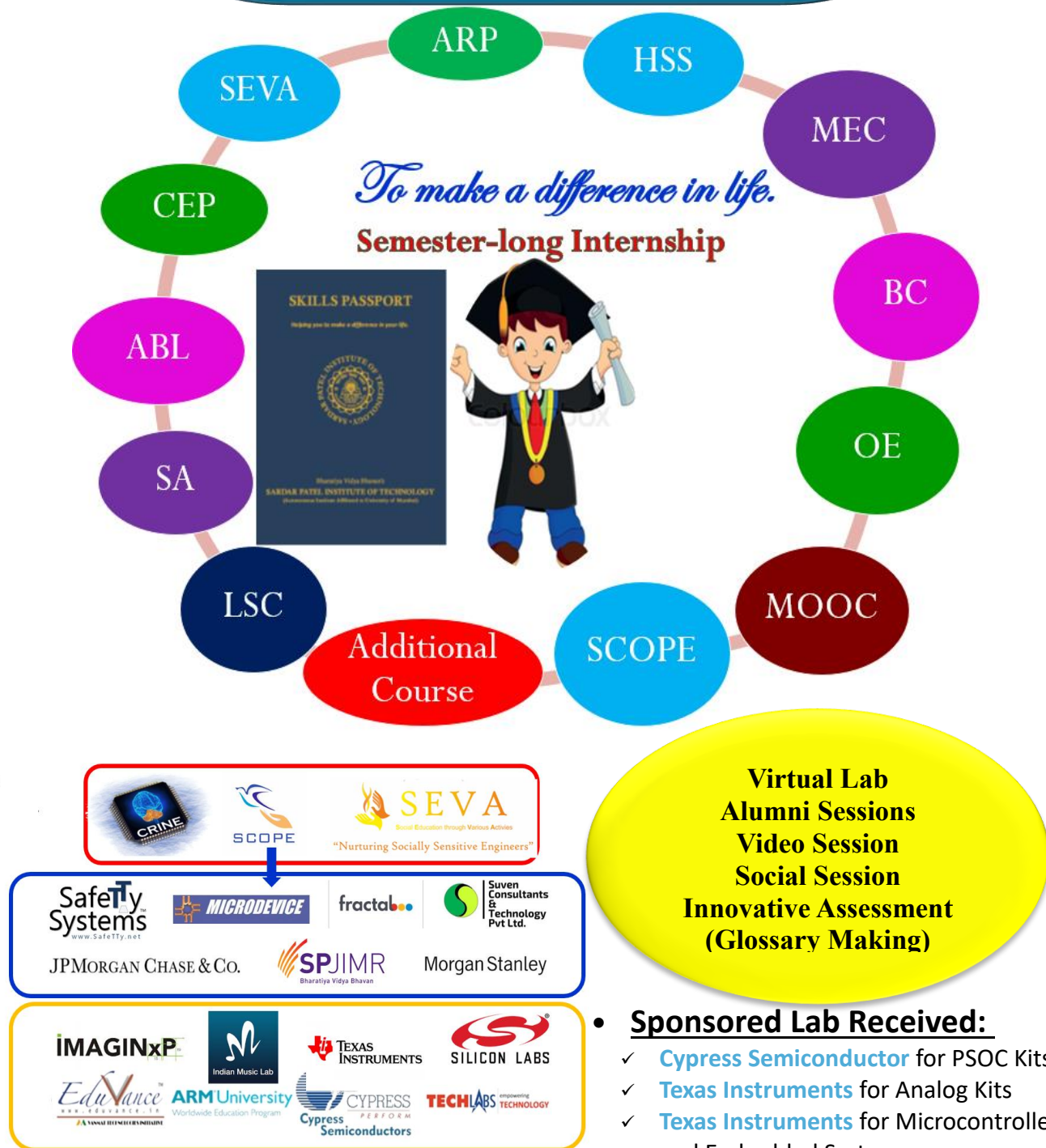
Surendra Rathod

4.2 ★★★★★ (2)

28.5 total hours • 92 lectures • Beginner

₹1,280

Academic Innovations



• MoU Signed:-

- ✓ **ImaginXp** for Post Graduate Diploma Program in User Experience
- ✓ **Fontys University** of Applied Sciences, School of ICT, The Netherlands for Student Exchange
- ✓ **Eduvance** for Lab Set-ups
- ✓ **Cogenda Singapore** for research collaboration
- ✓ **Credit Suisse** for SCOPE program
- ✓ **FSAI** for Fire, Safety and Automation Training

• Sponsored Lab Received:

- ✓ **Cypress Semiconductor** for PSOC Kits
- ✓ **Texas Instruments** for Analog Kits
- ✓ **Texas Instruments** for Microcontrollers and Embedded Systems
- ✓ **Texas Instruments** for Power Electronics
- ✓ **Silicon Labs** for Mixed Signal Controllers

Major Administrative Responsibilities

Organization	Designation	From	To	No. of Sem	Nature of Work
SPIT	Member of GB	01-01-2017	30-06-2022	9	Participation in Policy Decision Making
Bhavan's College	Management Representative on GB and CDC	27-11-2019	Till Date	7	Participation in Policy Decision Making
SPIT	Dean Academics (Member Secretary Academic Council)	01-01-2017	20-08-2019	5	Design and implementation of curriculum and evaluation system
SPIT	NBA Coordinator (Institute Level)	10-11-2011	01-01-2017	10	NBA accreditation related work
SPIT	Head of Department	10-11-2011	19-08-2019	17	Administration of Department
SPIT	Chairman DAB and BoS	01-07-2012	20-08-2019	16	Academic planning related work
SPIT	Admission Committee Chair	2021 & 2022	Till Date	2 Yr	Planning & Execution of F Y BTech admissions
SPIT	Convener	01-01-2017	Till Date	7	Grievance Committee
SPIT	Member Exam Committee	01-01-2017	19-08-2019	5	Exam related work
SPIT and VJTI	RRC Member	30-06-2013	Till Date	10	PhD research committee member, assessment etc
Mumbai University	Committee Chairman/ member	01-07-2011	30-05-2017	14	Curriculum design, Local Inquiry, paper setting, Member of staff selection committee, PhD Viva-Voce Examinations
Maharashtra Public Service Commission (MPSC)	Member Staff Selection Committee	01-07-2014	31-12-2019	2	Interview Panelist for MPSC recruitments
Many engineering colleges (FCRIT, SIES, CRCE, KCCoE, RGIT, AIKTC etc.)	Academic Auditor, DAB Member	2015	Till date		Department Academic audit
Industries: Eduvance and Vanmat Technologies	National Advisory Panel	2014	Till date		Deliberations on EdTech Products

Few of the Honors and Awards

- 1) Received '**ISTE Best Engineering College Teacher Award for Maharashtra State**' in year 2012.
- 2) Received recognition as IUCEE (Indo Universal Collaboration for Engineering Education) Faculty Fellow for the year 2016.
- 3) Awarded as a **Distinguished Professor by Computer Society of India (CSI)** for successfully demonstrating innovative and outstanding teaching methodology, organized by IITB, 2017.
- 4) Awarded as a **Distinguished HOD by Computer Society of India (CSI)** for successfully demonstrating innovative and outstanding teaching methodology, organized by IITB, 2017.
- 5) Received '**Outstanding Achievement Award**' for year 2007 by **Energy Society of India and College of Engineering Pondicherry** by his Excellency, **Government of Pondicherry**.
- 6) Awarded as '**Best Professor in Electronics Engineering**' at **10th DNA Innovative Education Leadership Award** organized by DNA and STARS Group.
- 7) Felicitated with **Vocational Excellence Award 2020** by **Rotary Club** of Mumbai West Coast
- 8) Received '**Shiksha Rattan Award**' and '**Certificate of Excellence**' in year 2012 by **International India Friendship Society, New Delhi** from **Mr. G. V. G. Krishnamoorthy (former Election Commissioner Govt. of India), Mr. Joginder Singh (CBI Director) and Mr. Ved Prakash (AICC Secretary)**.
- 9) Won **First Prize** for the Paper Titled "Single Event Upset Study of Helium and Argon on P+/EPI/N+ and SRAM Structure" in the **National Conf.**, Mumbai on 14th March 2009.
- 10) Won **Best Paper Award** for the Paper Titled "VLSI Implementation of a Viterbi Decoder" in the **National Conf.** held at **Government College of Engineering, Aurangabad** on 23rd & 24th Jan 2006.
- 11) Won **Best Paper Award** for the Paper Titled "Design and Simulation of PC to SRAM Interface for Reconfigurable Processors" in the **National Conf.** held at **MIT, Manipal** on 11th & 12th Nov 2005.
- 12) Prize winner in Project/Competition by **Institution of Engineers (India)** held at Nagpur on 16th and 17th March 1997.

Details of Doctoral Thesis Supervised

1. Approved Ph.D. guide of Mumbai University for Electronics Engineering since 2015.
2. Approved Ph.D. guide of Mumbai University for Electronics & Telecommunication Engineering since 2013.

Ph.D. Guided: Total=03

Name of Research Scholar	Title of Ph.D.	Year of Completion
Mr. Pramod Bhavarthe	Design of Compact Electromagnetic Band Gap Structures for Enhancement of Microstrip Patch Performances	2019
Mrs. Reena Sonkusare	Analysis of FinFET for analog performance and its application in analog circuit	2019
Mrs. Sushma Srivastava	Modeling of CNFET Based Neuromorphic Circuits	2019

Present Research Scholars: Total=05

S.N.	Name of Research Scholar	Title of Ph.D.
1	Mrs. Manisha Bansode	Design of Compact Electromagnetic Bandgap Structures for High Speed Signaling
2	Mrs. Payal Shah	Modeling and Design of Silicon Neurons and Synapse for Neuromorphic Chip Implementation
3	Mr. Vijay Kapure	Design of Metamaterial Structure for Triple Band-notch Ultrawideband Monopole Antenna
4	Mrs. Vidya Keshwani	Design of Compact Monopole Antenna with Low Specific Absorption Rate using Metamaterial
5	Mrs. Sejal Kadam	Investigation of 5G massive MIMO system performance with low resolution ADC and mixed ADC architectures

In last one year, PhD thesis are evaluated and worked as examiner for viva voce from RTM Nagpur University, Anna University, RK University, MG University Kerala, Punjab University etc. Also worked as Chairman for online Viva-voce PhD examination of two candidates of Mumbai University.

Reviewed research papers in many International Journals and conferences (VDAT NIT Surat, IBSSC IIIT Gwalior, TRIBES IIIT Raipur, ICF-CEET, ICAC3 etc.) Session Chair at TRIBES Raipur and Keynote speaker at ICF-CEET.

Grant Received

1. Mumbai University Minor Research Grant of Rs. 30,000/-- for the project "Determination of Water Quality Parameters" in year 2016-17.
2. Mumbai University Minor Research Grant of Rs. 35,000/-- for the project "Labview Based Online Pressure Monitoring System" in year 2013-14.
3. AICTE grant of Rs. 6.9 Lakhs for FDP on 'Electronic System Design: From devices to applications' in year 2014-15.
4. AICTE grant of Rs. 1 Lakh for National Seminar on 'Technologies for Development of Rural Areas' in year 2017-18.
5. AICTE-ISTE grant of Rs. 3 Lakhs for FDP on 'Innovative Teaching Learning Practices to Achieve Outcome Based Education and Accreditation' in year 2017-18.
6. AICTE grant of Rs. 3.62 Lakhs for STTP on 'Front End VLSI Design and Verification' in the Financial year 2018-19.
7. AICTE grant of Rs. 5.32 Lakhs for FDP on 'Consumer Electronic Product Design, Testing, Reliability and Patenting' in the Financial year 2018-19.
8. Mumbai University Minor Research Grant of Rs. 25,000/-- for the project "Automatic Umbrella Dryer" in year 2019-20.
9. AICTE grant of Rs. 5.63 Lakhs for Two Week FDP on 'Insights into Intelligent Automation, Machine Learning and Data Science' in the Financial year 2019-20. (Ref. No. 34-67/17/FDC/FDP/ P-1/2019-20 dated 30-06-2020) [Three Two Week Online FDPs are conducted
 1. FDP1-Foundations of data science: 19/10/2020 to 31/10/2020
 2. FDP2-Machine learning and artificial intelligence: 17/11/2020 to 29/11/2020
 3. FDP3-Data science and its applications: 07/12/2020 to 19/12/2020]
10. AICTE grant of Rs. 3.00 Lakhs for One Week STTP on 'VLSI Design Using Cadence Tools' in the Financial year 2020-21. (Ref. No. 34-65/345/RIFD/STTP/Policv-1/2018-19 dated 10-01-2020) [Three One Week Online STTPs are conducted
 1. STTP1-Digital design and verification: 12/10/2020 to 17/10/2020,
 2. STTP2-Analog CMOS VLSI Design: 02/11/2020 to 07/11/2020,
 3. STTP3-Mixed Signal CMOS VLSI Design: 30/11/2020 to 05/12/2020]
11. Funds received from various companies for ICCICT-2021 international conference as a 'Sponsorship Chair'. Quantiphi=Rs 1,00,000/--, Mathworks Inc=Rs 25000, Suven Consultants= Rs. 18,000/-- Microdevice Technologies= In kind around 1 lakh and technical sponsorship from companies like Barclays, J.P.Morgan etc.

Book Chapter Published: Gaurav Kaushal, Surendra S. Rathod, Ch Naga Raghuram, Sudeb Dasgupta, "Radiation hard circuit design: flip-flop and SRAM" chapter 12 in IET book "VLSI and Post-CMOS Electronics. Volume 2: Devices, circuits and interconnects" doi:10.1049/PBCS073G_ch12

Sample 5 Publications: Ph.D.

1. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Modeling of Threshold Voltage, Mobility, Drain Current and Sub-threshold Leakage Current in Virgin and Irradiated Silicon-on-Insulator Fin-Shaped Field Effect Transistor Device," *AIP Journal of Applied Physics*, vol. 109, no. 8, pp. 084504-1-11, Apr. 2011.
2. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Comparative Analysis of SEU in FinFET SRAM Cell's for Super-Threshold and Sub-Threshold Supply Voltage Operation," *IEEE Trans. on Electron Devices*, vol. 58, no. 10, pp. 3630-3634, Oct. 2011.
3. Gaurav Kaushal, S. S. Rathod, Satish Maheshwaram, S. K. Manhas, A. K. Saxena, and S. Dasgupta, "Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD SimAnnexureulation Study," *IEEE Trans. on Electron Devices*, vol. 59, no. 5, pp. 1563-1566, May 2012.
4. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "A Proposed DG-FinFET based SRAM cell Design with RADHARD Capabilities," *Elsevier Microelectronics Reliability*, vol. 50, no. 8, pp. 1181-1188, Aug. 2010.
5. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Electrical Performance Study of 25 nm Ω -FinFET under the Influence of Gamma Radiation: A 3D Simulation," *Elsevier Microelectronics Journal*, vol. 42, no. 1, pp. 165-172, Jan. 2011.

Sample 5 Publications: Post-Ph.D.

1. Reena Sonkusare, Omkar Joshi and S. S. Rathod "SOI FinFET Based Instrumentation Amplifier for Biomedical Applications," *Elsevier Microelectronics Journal*, vol. 91, no. 1, pp. 1-10, Sept. 2019.
2. Pramod P. Bhavarthe, Surendra S. Rathod, and K. T. V. Reddy, "A Compact Dual Band Gap Electromagnetic Band Gap Structure," *IEEE Trans. on Antennas and Propagation*, Vol. 67, No. 1, pp. 596-600, Oct. 2018.
3. Pramod Bhavarthe, Surendra Rathod and K.T.V. Reddy, "A Compact Two Via Hammer Spanner type Polarization Dependent Electromagnetic Band Gap Structure," *IEEE Microwave and Wireless Components Letters*, Vol. 28, No. 4, pp. 284-286, Apr 2018.
4. Pramod Bhavarthe, Surendra Rathod and K.T.V. Reddy, "Parametric Study for Rectangular Patch Antennas," *IEEE Microwave and Wireless Components Letters*, Vol. 27, No. 5, pp. 446-448, May 2017.
5. Reena Sonkusare, P. Pilankar and S. S Rathod, "Analysis of subthreshold SOI FinFET based two stage OTA for low power," *Springer Analog Integrated Circuits and Signal Processing*, Vol. 96, pp. 1-13, Aug 2018

Monogram: Authored 'Domains of Learning' in eBook 'Understanding Outcome Based Education and Accreditation' Published by State Project Implementation Unit (SPIU)-Uttar Pradesh and Institute of Engineering and Technology Dr. Bhimrao Ambedkar University

Patents Published

1. Patent Title: VEHICLE EVENT RECORDER AND CRASH RECOVERY SYSTEM

Inventor: Kankonkar Prateek, Ghadi Ameya, Patil Parth and Surendra Rathod

Application No: 816/MUM/2015 , Date of filing of Application: 13/03/2015 ,

Publication Date: 17/11/2017

2. Patent Name: A SYSTEM FOR RECORDING AND DISPLAYING.

Inventor: Malia Viraj, Gala Jugal, Gupta Samiksha, Surendra Rathod

Application No.4485/MUM/2015 , Date of filing of Application:30/11/2015 ,

Publication Date: 02/06/2017

3. Patent Name: ULTRASONIC BROADBAND GENERATOR

Inventor: Vakadkar Amogha, Rege Kunal, Thakur Rohan, Bhataria Manoj and Surendra Rathod,

Application No.1401/MUM/2013, Date of filing of Application: 13/03/2015,

Publication Date: 28/04/2017

4. A SYSTEM AND METHOD FOR ELECTRONIC SIGNATURE STAMP

Inventor: Kharade Sanish, Kumar Amit, Mukne Ankita, Rathod Surendra

Date of filing of Application: 13/06/2019

5. SYSTEM AND METHOD FOR UNASSISTED SEGREGATION OF PARCELS AND MAINTAINING THEIR TIME/DATE RECORDS AT POST OFFICES

Inventor: Gupta Shreya, Dongre Isha, Govindayapalli Manasvi, Rathod Surendra

Date of filing of Application: 13/06/2019

6. ELECTROMECHANICAL SYSTEM FOR SEGREGATION AND RECOVERY OF PLASTIC FROM SAND BEACH

Inventor: Rathod Surendra, Haldankar Govind, Bhat Bhardwaj, Bath Tejveer Singh, Dhar Gopala, Bhattacharjee Soumyadeb, Mainkar Yash, Gokhale Rutuja

Application No.202021010812, Date of filing of Application: 13/03/2020,

Publication Date: 02/04/2021

7. INTELLIGENT CONTROL SYSTEM TO DELIVER WATER FOR BATHING

Inventor: Rathod Surendra and Dave Jenil

Application No: 202221002564 Date of filing Application: 17/01/2022

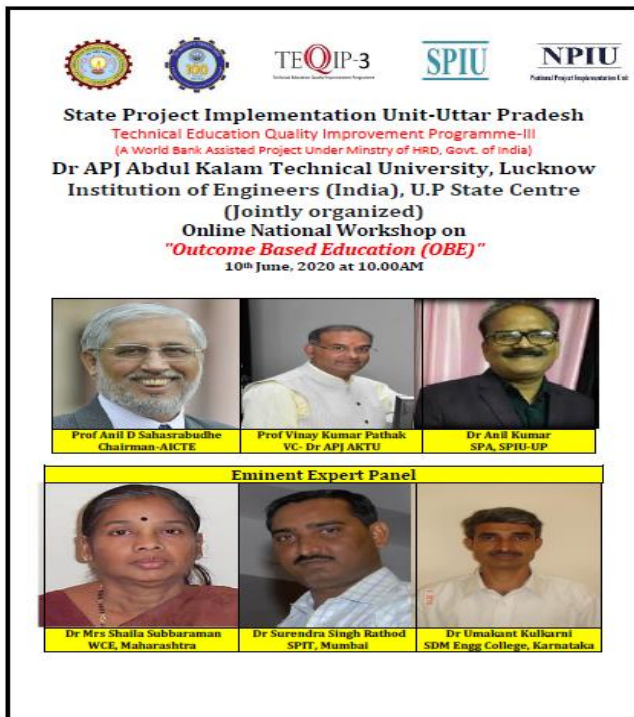
8. AI POWERED SINGLE SWITCH BASED REMOTE HEALTH MONITORING SYSTEM FOR ELDERLY

Inventor: Rathod Surendra and Kalbande Dhananjay

Application No: 202321008008, Date of filing Application: 08/02/2023

Publication Date: 03/03/2023

Other Engagements



Felicitations of SPIT FSAI Student Chapter member during FSIE at Bombay Exhibition Center, Goregaon for recognizing their efforts for Ganesh Mandal Audit



**Meeting with Governor of Nagaland
Hon. Shree Padmanabha Acharya**



**Interaction with AICTE Chairman
Dr. Anil Sahastrabudhe**



Meeting on lunch hosted by Mr. Aditya Thakre regarding discussion on plastic ban and garbage issue.



Meeting with Alumni at Deloitte, Hyderabad



MoU signed with Credit Suisse for CS Lab Program Under SCOPE initiative.



Meeting with Delegation from Netherlands about student exchange.



AMDOCS for discussion on SCOPE and Semester long internship.



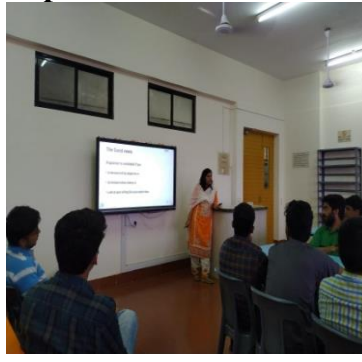
Visit at Barclays for discussion on SCOPE and Semester long internship.



Sparrow Day Celebration.



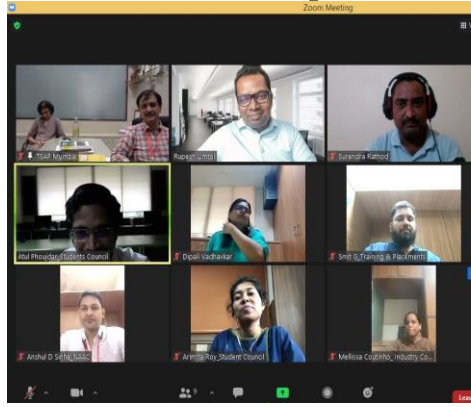
Flip Class Room Infra.



Rashtriya Ekta Diwas Celebration



Thakur School of Architecture, for FSAI Student Chapter



Finolex Academy of Management and Technology, Ratnagiri for FSAI Student Chapter installation.



SEVA Activity after Ganesh Visarjan



SEVA Activity (Every Sat & Sun Beach Cleaning, Mithi River Cleaning, Circular Economy and School Education)



Tree Plantation



Tree Plantation at Dahanu (300 Trees Planted this year)



Series of FY B.Tech Admission Counselling Webinars Arranged

SARDAR PATEL INSTITUTE OF TECHNOLOGY
Mumbai Nagar, Andheri (West), Mumbai 400 052

COUNSELLING FOR 12TH STANDARD STUDENTS ON ENGINEERING ADMISSION
Webinar on Placements, Internship and Entrepreneurship at S.P.I.T.

EVENT DETAILS
S.P.I.T. is known for kind of placements, internships & entrepreneur opportunities for students. This webinar is arranged to make prospective students aware about the meticulous efforts of our placement team for bringing a pool of career opportunities and skill building initiatives for students in making them successful technocrats.

Speakers

 Dr. Bhaskar Chaudhari President	 Dr. Dhananjay Rathore Dean	 Mr. Hrish Matreja FSAI President
 Dr. Surendra Rathore Chairman	 Prof. Kiran Talele Dean	 Mr. Vivek Mandali FSAI
 Mr. Vinod Bilka Placement and Recruitment Officer	 Mr. Mohit Joshi Alumni	 Ms. Vandana Vatsara FSAI

Youtube Link: shorturl.at/pCFF2

Time: 6:00 PM to 7:30 PM

Date: Saturday, 9th Oct 2021

Audience: Parents and Students

For more information log on to <https://www.spit.ac.in/admissions/>

QR Code



गणेश भक्तांना सुरक्षा पुरविणाऱ्या गणेश मंडळांना सेवाभावी संस्थांकडून पुरस्कार

मुंबईतील ८६० गणेश मंडळांचा सहभाग

मुंबई, दि. २२ (प्रतिनिधी) : सार्वजनिक गणेशोत्सवासाठी देशभरातून मुंबईत भाविक येत असतात. या नागरिकांच्या सुरक्षेसाठी पोलीसांसह इतर सर्व यंत्रणा सजज असतात, मात्र सर्वाधिक काळ मंडळांच्या मंडपांमध्ये असलेल्या या भाविकांच्या सुरक्षेसाठी तेथील सुरक्षेवाते अधिक सज्ज असणे आवश्यक आहे. मुंबईतील गणेश मंडळे भाविकांच्या सुरक्षेसाठी दृष्टीकोनातून आधुनिक तंत्रज्ञानाचा वापर करून अनेक चांगले उपक्रम राबवीत असून आगोष्ण घटना टाळण्यासाठी 'फायर अँड सिव्क्युरिटी असोसिएशन ऑफ इंडिया' या सेवाभावी संस्थेचे त्यांना सहकार्य लाभत आहे. 'फायर अँड सिव्क्युरिटी असोसिएशन ऑफ इंडिया' ही सेवाभावी संस्था गेली ७ वर्षे मुंबईतील गणेश मंडळांसेबत समन्वय साधून मुंबई पोलीस व मुंबई अग्नीशमन दल यांच्या मदतीने गणेश मंडळांचे सुरक्षा ऑडिट करीत आहेत. यांच्या स्फोटका सीसीटीव्ही कॅमेरा लावणे, आग विखण्याच्या साधनांची तपासणी, मेटल डिटेक्टर सुरक्षा यंत्रणा, अशा अनेक बाबींचा विचार करून हे सेप्टी ऑडिट राबविले जाते.



फायर अँड सिव्क्युरिटी असोसिएशन ऑफ इंडिया मुंबई चॅप्टरचे अध्यक्ष अश्विन ईशंतकर यावेळी बोलताना म्हणाले, 'उत्सवादरम्यान जर कोणतीही आपत्कालीन परिस्थिती उद्भवली तर सरकारी यंत्रणांची मदत पोहोचण्यात बचाव कार्य करणे करायचे याबाबत कार्यकर्ते प्रशिक्षित असणे आवश्यक आहे. आमची संस्था २००२ सालापासून फायर प्रोटेक्शन, लाइफ सेफ्टी, सिव्क्युरिटी, बिल्डींग अँटिमेशन, लॉस प्रिव्हेंशन आणि रिस्क मॅनेजमेंट या क्षेत्रात सक्ती संस्थांसेबत काम करीत आहे. मुंबईत तीन हजारहून अधिक गणेश मंडळे असून दरवर्षी गणेशमूर्ती पाहण्यासाठी पर्यटक व भाविकांची गर्दी वाढतच आहे. आमच्या संस्थेची संपूर्ण भारतभर २३ हून अधिक चॅप्टर असून मुंबईतील या सामाजिक उपक्रमाचे आठवे वर्ष असून गेल्यावर्षी २५० मंडळांनी यात सहभाग घेतला होता याबवी आम्ही ८६० गणेश मंडळांचे रजिस्ट्रेशन केले आहे मुंबईतील नावाजलेल्या गणेश मंडळांकडून आम्हाला सकारात्मक प्रतिसाद लाभत आहे.

प्रातःकाल Sun, 23 September 2018
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Navya Navelli Nanda (Grand daughter of Shri Amithabh Bachhan) to collaborate with Nimaya Foundation



Walkathon Water Bowl Challenge Launch & Animal Health Camp with Actress Bhumi Pednekar and Priya Agarwal Hebbar Ex Director Vedanta Ltd.



With Ms. Shareen Kitterman, US Diplomat during Annual Day



Alumni Actor Ms. Suchitra Pillai during alumni meet



With Prof. V. N. Rajasekharan Pillai Vice Chancellor of Somaiya Vidyavihar University during Degree Distribution



With Mr. Siddhartha Jadhav, Actor during Ganesh Mandal Audit by FSAI at Ganeshgalli Lalbaugh Sarvajani Utsav



Dr. Jayanthi Murthy, President of Oregon University, USA.



With Dr Abhay Wagh, Director DTE Maharashtra State.



With Dr Karbhari Kale, Vice Chancellor of Dr. Babasaheb Ambedkar University Lonere.



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