Lesson Plan

Faculty: Sangeeta Parshionikar

CLASS	SE Electronics, Semester III
Academic Term	July – November 2020
Subject	**Digital Electronics (ECC303)**

Periods (Hours) per week	***Lecture***	***4***	
	Practical	***8***	
	Tutorial	***--***	
Evaluation System		***Hours***	***Marks***
	Theory examination	3	80
	Internal Assessment	--	20
	Practical & Oral Examination	--	25
	Term work	--	25
	Total	--	150

Time Table	***Day***	***Time***
	Monday	10 – 11 am
	Tuesday	9 – 10 am
	Wednesday	12.30 – 1.30 pm
	Friday	10 – 11 am

Course Content and Lesson plan

Module 1- **Fundamentals of Digital Design**

Week	Lecture No.	Date		Topic	Ref.	Remar-ks
		Planned	**Actual**			
1	1	10-07-2020	10-07-2020	**Number Systems and Codes-** Review of Number System, Decimal, Binary, Octal, Hexdecimal number system	**1,2**	
2	2	13-07-2020	13-07-2020	Binary Code, Binary Coded	**1,2**	

				Decimal, Octal Code, Hexadecimal Code		
	3	14-07-2020	14-07-2020	Code and their conversions, Decimal to binary, Octal, Hexadecimal and vice versa	**1,2**	
	Quiz 1 – Number Conversion				**Date: 14th July 2020**	
	4	15-07-2020	15-07-2020	Binary Arithmetic: One's and two's complements,	**1,2**	
2	5	17-07-2020	17-07-2020	Excess-3 Code, Gray Code	**1,2**	
3	6	20-07-2020	20-07-2020	Weighted code, Parity Code: Hamming Code	**1**	
	7	21-07-2020	21-07-2020	Digital logic gates, AND, OR, NOT, Universal Gates NAND, NOR gates	**1,2**	
	8	22-07-2020	22-07-2020	Realization using NAND, NOR gates, Boolean Algebra, De Morgan's Theorem	**1,2**	
	9	24-07-2020	24-07-2020	SOP and POS representation	**1,2**	
4	10	27-07-2020	27-07-2020	K Map up to four variables	**1,2**	
	11	28-07-2020	28-07-2020	Design of Boolean functions using Nand Nor gates only		
Quiz 2: Design 4 bit Binary to Gray Code converter.					**Date: 28th July 2020**	
	12	29-07-2020	29-07-2020	Hamming Code: Error Detection & correction code	**1,2**	
Assignment I - Fundamentals of Digital Electronics **Given Date: 31/07/2020**				**Submission Date: 07/08/2020**		
***Module 2* - Combinational Circuits using basic gates as well as MSI devices**						
	13	31-07-2020	31-07-2020	Half adder, Full adder, Ripple carry adder	**1,2**	
5	14	03-08-2020	03-08-2020	Carry Look ahead adder,		
	15	04-08-2020	04-08-2020	Half Subtractor, Full Subtractor, multiplexer	**1**	
	16	05-08-2020	05-08-2020	cascading of Multiplexer, demultiplexer	**1**	
	17	07-08-2020	07-08-2020	decoder, Comparator (Multiplexer and demultiplexer gate level upto 4:1).	**1,4**	
6	18	10-08-2020	10-08-2020	MSI devices - IC 7483, IC 74151, IC 74138, IC 7485	**1,4**	

	19	11-08-2020	11-08-2020	Magnitude Comparators, BCD Adder		
Quiz 3: Design of Boolean equation using Multiplexer. Date : 11 August 2020						
	20	12-08-2020	12-08-2020	Decoder 4:1, Decoder design		
***Module6* – Introduction to Verilog HDL**						
	21	14-08-2020	14-08-2020	Introduction to Hardware Description Language and its core features, synthesis in digital design	**3**	
7	22	17-08-2020	17-08-2020	Logic value system, data types, constants, parameters, wires and registers	**3**	
	Quiz 4: Design 4 bit BCD adder using IC 7438. Date : 17 August 2020					
	23	18-08-2020	18-08-2020	Logical, arithmetic, relational, shift operator	**3**	
	24	19-08-2020	19-08-2020	always, if, case, loop statements,	**3**	
	25	21-08-2020	21-08-2020	Gate level modelling, Module instantiation statements.	**3**	
8	26	24-08-2020	24-08-2020	Combinational logic eg. Arithmetic circuits, Multiplexer, Demultiplexer, decoder	**3**	
	27	25-08-2020	25-08-2020	Continuous & procedural assignment statements	**3**	
	28	26-08-2020	26-08-2020	Simulation Edaplayground	**3**	
9	29	31-08-2020	31-08-2020	Sequential logic eg. flip flop, counters	**3**	
	30	01-09-2020	01-09-2020	Behaviral modeling og Verilog	**3**	
	31	02-09-2020	02-09-2020	Revision of Basics of Verilog	**3**	
Quiz 5: Quiz on Verilog Date 07 September 2020						
Module 3 - Elements of Sequential Logic Design						
	32	04-09-2020	04-09-2020	Latches and Flip-Flops. RS	**1,7**	
10	33	07-09-2020	07-09-2020	JK and Master slave flip flops	**1,7**	
	34	08-09-2020	08-09-2020	T & D flip flops with various triggering methods	**1,7**	
	35	09-09-2020	09-09-2020	Conversion of flip flops	**1,7**	
	36	11-09-2020	11-09-2020	Asynchronous, Up Down Counters.	**1,7**	
Unit Test 1 : Date: 16 September 2020						
11	37	22-09-2020	22-09-2020	Asynchronous, Up Down	**1,7**	

				Counters using different FF		
	38	23-09-2020	23-09-2020	Synchronous Counters,		
	39	25-09-2020	25-09-2020	Modulus Counters,		
12	40	28-09-2020	28-09-2020	Ring Counter, Twisted ring counter		
	41	29-09-2020	29-09-2020	Shift Registers, Universal Shift Register		
Module 4 - Sequential Logic Design						
	42	30-09-2020	30-09-2020	Mealy and Moore Machines	**2,1,7**	
	43	02-10-2020	02-10-2020	Clocked synchronous state machine analysis	**2**	
	44	05-10-2020	05-10-2020	State reduction techniques (inspection, partition and implication chart method) and state assignment	**2**	
	45	06-10-2020	06-10-2020	sequence detector, Clocked synchronous state machine design	**2**	
13	46	07-10-2020	07-10-2020	MSI counters (7490, 7492, 7493,74163, 74169) and applications	**2**	
	47	09-10-2020	09-10-2020	MSI Shift registers (74194) and their applications	**2**	
Module 5 - Logic Families and Programmable Logic Devices						
14	48	12-10-2020	12-10-2020	Types of logic families (TTL and CMOS), characteristic parameters - propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in	**6**	
	49	13-10-2020	13-10-2020	transfer characteristics of TTL NAND Operation of TTL NAND gate	**6**	
	50	14-10-2020	14-10-2020	CMOS Logic: CMOS inverter, CMOS NAND and CMOS NOR, Interfacing CMOS to TTL and TTL to CMOS	**6**	
	51	16-10-2020	16-10-2020	Concepts of PAL and PLA. Simple logic implementation using PAL and PLA	**6**	
15	52	19-10-2020	19-10-2020	Introduction to CPLD and FPGA architectures	**6**	
	53	20-10-2020	20-10-2020	Numericals based on PAL and PLA	**6**	

	54	21-10-2020	21-10-2020	**Revision of** Mealy Moore machine Unit 4	**1,2,7**	
Flipped class activity						
13	55	23-10-2020	23-10-2020	Sequence Detector	**1,2**	
	56	26-10-2020	26-10-2020	Sums on Sequence Detector	**1,2**	
	57	27-10-2020	27-10-2020	Flipped class activity		
	58	28-10-2020	28-10-2020	Practical Session		
17	59	30-10-2020	30-10-2020		**Eid – a -Milad**	
	60	02-11-2020	02-11-2020	Seminars by Students		
	61	03-11-2020	03-11-2020	Revision sums on Synchronous Counter		
	62	06-11-2020	06-11-2020	PLA & PAL Revision		
Total	**62**					

Text Books:

1. R. P. Jain, Modern Digital Electronics, Tata McGraw Hill Education, Third Edition 2003.
2. Morris Mano, Digital Design, Pearson Education, Asia 2002.
3. J. Bhaskar, A Verilog HDL Primer, Third Edition, Star Galaxy Publishing, 2018.

Reference Books:

1. Digital Logic Applications and Design – John M. Yarbrough, Thomson Publications, 2006
2. John F. Warkerly, Digital Design Principles and Practices, Pearson Education, Fourth Edition, 2008.
3. Stephen Brown and Zvonko Vranesic, Fundamentals of digital logic design with Verilog design, McGraw Hill, 3rd Edition.
4. Digital Circuits and Logic Design – Samuel C. Lee, PHI
5. William I.Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India.
6. Parag K Lala, "Digital System design using PLD", BS Publications, 2003.
7. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

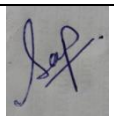
Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks.

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.

3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.

• **Submitted By**	**Approved By**
Prof. Sangeeta Parshionikar 	**Prof. Shilpa Patil**
Sign:	Sign:
Date of Submission: 06/07/2020	**Date of Approval:**
Remarks by PAC (if any)	