**Course Plan**

**T.E. (ECS) (Semester V)**

**Computer Organization and Architecture**

**Subject code: ECC 502**

**Teacher-in-charge: Dr. Sapna Prabhu Academic Term: July-October 2022**

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| --- | --- | --- | --- |
| **Module****No.** | **Unit No.** | **Contents** | **Hrs.** |
| **1** |  | **Introduction to Computer Organization** | **02** |
| **1.1** | Fundamental Units of a Computer, Basic Measures of Computer Performance - Clock Speed, CPI, MIPs and MFlops |
| **1.2** | Number Representation methods- Integer and Floating-point |
| **2** |  | **Processor Organization and Architecture** | **05** |
| **2.1** | CPU Architecture, Register Organization, Instruction cycle, Instruction Formats |
| **2.2** | Control Unit Design- Hardwired and Micro-programmed Control: Vertical and Horizontal Micro-Instructions, Nano-programming |
| **2.3** | Comparison between CISC and RISC architectures |
| **3** |  | **Memory and I/O Organization** | **09** |
| **3.1** | Classification of Memories-Primary and Secondary Memories, ROM and RAM, Memory Inter- leaving |
| **3.2** | Memory Hierarchy, Cache Memory Concepts, Mapping Techniques, Write Policies, Cache Coherency |
| **3.3** | Virtual Memory Management-Concept, Segmentation, Paging, Page Replacement policies |
| **3.4** | Types of I/O devices and Access methods, Types of Buses, Bus Arbitration |
| **4** |  | **Operating System concepts** | **15** |
| **4.1** | Concept of a Process, Process States, Process Description, Process Control Block |
| **4.2** | Process scheduling -Pre-emptive and Non pre-emptive scheduling algorithms (FCFS, Priority, SJF), Concept of Multi-Threading |
| **4.3** | Inter-Process Communication, Process Synchronization, Deadlock and Prevention |
| **4.4** | File Management -File Organization and Access |
| **4.5** | I/O Management and Disk Scheduling: FCFS, SSTF |
| **5** |  | **Parallelism** | **04** |
| **5.1** | Introduction to Parallel Processing Concepts, Flynn's classification, Amdahl's law |
| **5.2** | Pipelining - Concept, Speedup, Efficiency, Throughput, Types of Pipeline hazards and solutions |
| **6** |  | **Architectural Enhancements** | **04** |
| Superscalar Architectures, Out-of-Order Execution, Multi-core processors, Clusters, GPU |
| **Total** | **39** |

**Course Objectives:**

1. To introduce the learner to the design aspects which can lead to maximized performance of a Computer.

 2. To introduce basic concepts and functions of operating systems.

 3. To understand the concepts of process synchronization and deadlock.

4. To understand various Memory, I/O and File management techniques

5. To introduce the learner to various concepts related to Parallel Processing

6. To highlight the various architectural enhancements in modern processors

**Course Outcomes:**

**After successful completion of the course students will be able to:**

ECC 502 .1- Define the performance metrics of a Computer

ECC 502 .2- Explain the design considerations of Processor, Memory and I/O in Computer systems

ECC 502 .3- Interpret the objectives and functions of an Operating System

ECC 502 .4-Analyse the concept of process management and evaluate performance of process scheduling algorithms

ECC 502 .5-Evaluate the advantages and limitations of Parallelism in systems

ECC 502.6-Discuss the various architectural enhancements in modern processors

**CO-PO-PSO Mapping:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **ECC 502 .1** | 3 |  |  |  |  |  |  |  |  |  |  |  |
| **ECC 502 .2** | 2 | 3 |  |  |  |  |  |  |  |  |  |  |
| **ECC 502 .3** |  | 2 | 2 |  |  |  |  |  |  |  |  |  |
| **ECC 502 .4** |  | 2 |  | 2 |  |  |  |  |  |  |  |  |
| **ECC 502 .5** |  | 2 |  |  |  |  |  |  |  |  |  | 1 |
| **ECC 502 .6** |  | 2 |  |  |  |  |  |  |  |  |  | 1 |

**Provide justification of PO to CO mapping**

|  |  |  |
| --- | --- | --- |
| ECC 502 .1 | PO1 | Apply the knowledge of engineering fundamentals and an engineering specialization to the solution of complex engineering problems. |
| ECC 502 .2 | PO1 | Apply the knowledge of engineering fundamentals and an engineering specialization to the solution of complex engineering problems. |
| PO2 | Identify, formulate and analyze complex engineering problems reaching substantiated conclusions using first principles of engineering sciences. |
| ECC 502 .3 | PO2 | Identify, formulate and analyze complex engineering problems reaching substantiated conclusions using first principles of engineering sciences. |
| PO3 | Design solutions for engineering problems and design systemprocesses that meet the specified needs |
| ECC 502 .4 | PO2 | Identify, formulate and analyze complex engineering problems reaching substantiated conclusions using first principles of engineering sciences. |
| PO4 | Use research-based knowledge including analysis, and interpretation of data and synthesis of the information to provide valid conclusions |
| ECC 502 .5 | PO2 | Identify, formulate and analyze complex engineering problems reaching substantiated conclusions using first principles of engineering sciences. |
| PO12 | Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. |
| ECC 502 .6 | PO2 | Identify, formulate and analyze complex engineering problems reaching substantiated conclusions using first principles of engineering sciences. |
| PO12 | Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. |

**CO Assessment Tools:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Course Outcomes** | **Tests** | **Participation in Additional activities** | **End Semester****Examination** | **Course Exit Survey** |
|  | 1 | 2 |  |  |  |
| **ECC 502 .1** | 30% | - | 10% | 60% | 100% |
| **ECC 502 .2** | 20% | 10% | 10% | 60% | 100% |
| **ECC 502 .3** | - | 20% | 20% | 60% | 100% |
| **ECC 502 .4** | - | 20% | 20% | 60% | 100% |
| **ECC 502 .5** | - | 10% | 30% | 60% | 100% |
| **ECC 502 .6** | - | - | 40% | 60% | 100% |

**CO calculation= (0.8 \*Direct method + 0.2\*Indirect method)**

**Rubrics for assessing Course Outcome with each assessment tool**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Indicator** |  |  |  |  |
| Timeline (3) | More than two sessions late (0) | More than one session late (1) | One session late (2) | On time (3) |
| Depth of Understanding (4) | Unsatisfactory (1) | Superficial (2) | Satisfactory (3) | Adequate (4) |
| Completeness (3) | Not submitted (0) | Major topics are omitted or addressed minimally (1) |  Most major and some minor points are covered and are accurate (2) | All major and minor points are covered and are accurate (3) |

**Content beyond syllabus:**

1. Case Study on the Pentium Processor

2. Technical paper reading (Home activity)

3. Technical article discussion on “The Multiple lives of Moore’s Law "

**Modes of content delivery**

|  |  |
| --- | --- |
| **Modes of Delivery** | **Brief description of content delivered** |
| Class room lectures | Powerpoint presentations as well as White Board teaching was used. Videos to be used for certain topics |
| **Class discussions** | **1.Discussion on Technical article on “Moore’s Law”****2.Class discussion /debate on CISC Vs RISC Design Philosophy** |

**Text books:**

1. William Stallings, “*Computer Organization and Architecture: Designing for Performance*”, Eighth Edition, Pearson.

2. C. Hamacher, Z. Vranesic and S. Zaky, "Computer Organization", McGraw Hill,2002.

3. William Stallings, Operating System: Internals and Design Principles, Prentice Hall, 8th Edition

4. Abraham Silberschatz, Peter Baer Galvin and Greg Gagne, Operating System Concepts, John Wiley &Sons, Inc., 9th Edition

**Reference Books:**

1. P. Hayes, "Computer Architecture and Organization", McGraw-Hill,1998.

2. B. Govindarajulu, “*Computer Architecture and Organization: Design Principles and Applications*”, Second Edition, Tata McGraw-Hill.

3. D. A. Patterson and J. L. Hennessy, "Computer Organization and Design - The Hardware/Software Interface", MorganKaufmann,1998.

4. Achyut Godbole and Atul Kahate, Operating Systems, McGraw Hill Education, 3rd Edition

5. Andrew Tannenbaum, Operating System Design and Implementation, Pearson, 3rd Edition

**Lesson Plan**

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| **TE Electronics and Computer Science, Semester V** |
| **July-October 2022** |
| **Computer Organization and Architecture** **(ECC 502)** |
| **Lectures** | **3 per week** |
|  | **Hours** | **Marks** |
| Theory examination | 3 | 80 |
| Internal Assessment |  | 20 |
| Total | -- | 100 |
| **Day** | **Time** |
| Monday | 12 pm-1 pm |
| Wednesday | 1.30 pm-2.30 pm |
| Friday | 9.45 am-10.45 am |
| **Lecture No.** | **Dates** | **Topic** | **Remarks** |
| **Planned** | **Actual** |
| 1 | 18/7/2022 | 18/7/2022 | Introduction |  |
| 2 | 20/7/2022 | 20/7/2022 | History of Computers |  |
| 3 | 22/7/2022 | 22/7/2022 | Basic Measures of Computer Performance |  |
| 4 | 25/7/2022 | 25/7/2022 | **Class Discussion on IEEE article on: Moore’s Law”** |  **Beyond Syllabus Activity** |
| 5 | 27/7/2022 | 27/7/2022 | Fundamental Units in a Computer |  |
| 6 | 29/7/2022 | 29/7/2022 | Integer and Floating point representations |  |
| 7 | 1/8/2022 | 1/8/2022 | Processor Architecture |  |
| 8 | 3/8/2022 | 3/8/2022 | Single data-path organization |  |
| 9 | 5/8/2022 | 5/8/2022 | Control sequence |  |
| 10 | 8/8/2022 | 8/8/2022 | Register Organization |  |
| 11 | 10/8/2022 | 10/8/2022 | Instruction Cycle, Formats |  |
| 12 | 12/8/2022 | 12/8/2022 | Control Unit Design- Hardwired Control |  |
| 13 | 17/8/2022 | 17/8/2022 | Micro-programmed Control  |  |
| 14 | 19/8/2022 | 19/8/2022 | Vertical and Horizontal Micro-Instructions, Nano-programming |  |
| 15 | 22/8/2022 | 22/8/2022 | **Comparison between CISC and RISC architectures**  | **Class Discussion/ Debate** |
| 16 | 24/8/2022 | 24/8/2022 | Classification of Memories-Primary and Secondary Memories, ROM and RAM, **Memory Inter- leaving** |  |
| 17 | 26/8/2022 | 26/8/2022 |  Memory Hierarchy, Cache Memory Concepts |  |
| 18 | 29/8/2022 | 29/8/2022 | Mapping Techniques  | **Supplement with Online Video** |
|  | **Unit Test 1- September 7-9,2022** |
| 19 | 9/9/2022 | 9/9/2022 | Write Policies, Cache Coherency |  |
| 20 | 12/9/2022 | 12/9/2022 | Virtual Memory Management-Concept, Segmentation |  |
| 21 | 14/9/2022 | 14/9/2022 | Paging, Page Replacement policies |  |
|  | **Technical Paper Reading /Discussion** |
| 22 | 16/9/2022 | 16/9/2022 | **Types of I/O devices and Access methods, Types of Buses, Bus Arbitration**  | **Notes** |
| 23 | 19/9/2022 | 19/9/2022 | Concept of a Process, Process States, Process Description, Process Control Block  |  |
| 24 | 21/9/2022 | 21/9/2022 | Process scheduling  |  |
| 25 | 23/9/2022 | 23/9/2022 | Pre-emptive and Non pre-emptive scheduling algorithms (FCFS, Priority, SJF) |  |
| 26 | 26/9/2022 | 26/9/2022 | Concept of Multi-Threading |  |
| 27 | 30/9/2022 | 30/9/2022 | Inter-Process Communication, Process Synchronization |  |
| 28 | 3/10/2022 | 3/10/2022 | Deadlock and Prevention |  |
| 29 | 7/10/2022 | 7/10/2022 | File Management **-**File Organization and Access  |  |
| 30 | 10/10/2022 | 10/10/2022 | I/O Management and Disk Scheduling: FCFS, SSTF  |  |
| 31 | 12/10/2022 | 12/10/2022 | Parallel Processing Concepts, Flynn's classification, Amdahl's law  |  |
| 32 | 14/10/2022 | 14/10/2022 | Pipelining - Concept, Speedup, Efficiency, Throughput  |  |
| 33 | 21/10/2022 | 21/10/2022 | Types of Pipeline hazards and solutions |  |
| 34 | 21/10/2022 | 21/10/2022 | Superscalar Architectures, Out-of-Order Execution | **Extra Class** |
| 35 | 21/10/2022 | 21/10/2022 | Multi-core processors, Clusters, GPU  | **Extra class** |

**Examination Scheme**

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| --- | --- | --- | --- |
| Module | Lecture Hours | Marks distribution in Test (For internal assessment/TW) | Approximate Marks distribution in Sem. End Examination |
| Test 1 | Test 2 |
| 1 | Introduction to Computer Organization | 2 | 5 | - | 5 |
| 2 | Processor Organization and Architecture | 5 | 9 | - | 15 |
| 3 | Memory and I/O Organization | 9 | 6 | - | 20 |
| 4 | Operating System concepts | 15 | - | 10 | 25 |
| 5 | Parallelism | 4 | - | 5 | 8 |
| 6 | Architectural Enhancements | 4 | - | 5 | 7 |

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| **Submitted By**  | **Approved By** |
| Dr Sapna Prabhu  |  Prof. Shilpa Patil  |
| Sign: |  Sign: |
|  |  |
| **Date of Submission:** | **Date of Approval:** |
|  |
| **Remarks by PAC (if any)** |