FR. Conceicao Rodrigues College Of Engineering

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

Department of Electronics Engineering

Lecture Plan

Subject: VLSI Design (ELX603) Credits-6

T.E. (ELECTRONICS) (semester VI) (2018-2019)

1. Syllabus:

Module	Contents	Hours
1	**Technology Trend:** **1.1 Technology Comparison:** Comparison of BJT and CMOS technology **1.2 MOSFET Scaling:** Types of scaling, Level 1 and Level 2 MOSFET Models, MOSFET capacitances	6
2	**MOSFET INVERTERS:** **2.1 Types of MOS Inverters:** Active and passive load and their comparison **2.2 Circuit Analysis of MOSFET INVERTERS:** Static analysis of resistive load and CMOS inverter, calculation of all critical voltages and noise margins. Design of symmetric CMOS inverters, CMOS Latch-up **2.3 Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR and complex Boolean function using equivalent CMOS inverter for simultaneous switching.	10
3	**MOS Circuit Design Styles:** **3.1 Design Styles:** Static CMOS, pass transistor logic, transmission gate, Pseudo NMOS, Domino, NORA, Zipper, C2MOS **3.2 Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, decoder using above design styles	10
4	**Semiconductor Memories:** **4.1 SRAM:** SRAM operation, design strategy, leakage currents, read/write circuits), Sense amplifier **4.2 DRAM:** 1T_DRAM, operation modes, leakage currents, refresh operation, Input-Output circuits **4.3 ROM Array**: NAND and NOR PROM, Nonvolatile read/write memories classification and programming techniques	8
5	**Data Path Design:** **5.1 Adder:** Bit adder circuits, ripple carry adder, CLA adder , MODL, Manchester carry chain and high speed adders like carry skip, carry select and carry save. **5.2 Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, barrel shifter	4
6	**VLSI Clocking and System Design:** **6.1 Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution **6.2 Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling **6.3 IO pads and Power Distribution:** ESD protection, input circuits, output circuits, simultaneous switching noise, power distribution scheme **6.4 Interconnect:** Interconnect delay model, interconnect scaling and crosstalk	10

2. Course Outcomes:

Upon completion of this course students will be able to:

EXL603.1 Demonstrate a clear understanding of choice of technology, scaling, MOS models and system level design issues.

EXL603.2 Design and analyze MOS based inverter.

EXL603.3 Design MOS based logic circuits with different circuit design styles.

EXL603.4 Design semiconductor memories, adders and multipliers.

EXL603.5 Describe system level design issues such as protection, timing and power dissipation.

3. Relationship of course outcomes with program outcomes: Indicate LI (low importance), MI (Moderate Importance) or HI (High Importance) in respective mapping cell.

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
EXL603.1	**3**													**2**
EXL603.2		**2**	**1**	**2**										**2**
EXL603.3			**2**	**2**										**2**
EXL603.4	**3**			**2**										**2**
Course	**3**	**2**	**1.5**	**2**										

4. CO Assessment Tools:

Course Outcome	***Assessment Method***										
	Direct Method (80 %)										***Indirect Method (20%)***
	Unit Tests		Assignments		Quiz		Laboratory Practical	Mini Proj -ect	End Sem Exam		Course exit survey
	1	2	1	2	1	2			Th.	Oral	
EXL603.1	20%				20%		10%		30%	20%	100%
EXL603.2	20%		20%				10%		30%	20%	100%

EXL603.3		20%		10%			20%		30%	20%	100%
EXL603.4		20%				20%	10%		30%	20%	100%
EXL603.5								100%			

CLASS		TE Electronics, Semester VI	
Academic Term		Jan – Apl 2019	
Subject		**VLSI Design (EXL603)**	
Periods (Hours) per week	***Lecture***	***4***	
	Practical	***8***	
	Tutorial	***--***	
Evaluation System		***Hours***	***Marks***
	Theory examination	3	80
	Internal Assessment	--	20
	Practical Examination	--	--
	Oral Examination	--	25
	Term work	--	25
	Total	--	150
Time Table	***Day***	***Time***	
	Monday	8.45 – 9.45 am	
	Tuesday	9.45 – 10.45 am	
	Thursday	1.30 – 2.30 pm	
	Friday	8.45 – 9.45 am	

Course Content and Lesson plan

Module 1- Technology Trend

Week	Lecture No.	Date		Topic	Ref.	Remar-ks
		Planned	Actual			
1	1	01 – 01 – 19	01 – 01 – 19	Introduction to VLSI design, Discrete & Integrated circuits, Classification – SSI, MSI, LSI& VLSI. VLSI design flow	1	
	2	02 – 01 – 19	02 – 01 – 19	Revision of MOS Structure, Energy band diagram, Operating modes of MOSFET, I- V Characteristics, GCA, CLM.	1	
	3	03 – 01 – 19	05 – 01 – 19	Comparison of BJT, NMOS and CMOS technology	**1**	
	4	04 – 01 – 19	04 – 01 – 19	Need of Scaling, Types, Full and Constant Voltage Scaling, Their Advantages & Disadvantages	**1,2**	
2	5	07 – 01 – 19	07 – 01 – 19	MOSFET capacitances, Oxide and Junction Capacitances, Equivalent circuit.	**1,2**	
	6	08 – 01 – 19	08 – 01 – 19	Details of Level 1 and Level 2 MOSFET Models	**1,2**	
Module 2 – MOSFET Inverters						
	7	09 – 01 – 19	09 – 01 – 19	MOS Inverter basics, comparison of all types of MOS inverters.		
	8	10 – 01 – 19	10 – 01 – 19	**Quiz On 1st Module (20M)**		
	9	11 – 01 – 19	11 – 01 – 19	Analysis of Resistive MOS Inverter (V_{OH}, V_{OL}, V_{IH}, V_I calculation)		
3	10	14 – 01 – 19	14 – 01 – 19	Analysis of CMOS Inverter (V_{OH}, V_{OL}, V_{IH}, V_I calculation)	**1** **Video**	

	11	15 – 01 – 19	15 – 01 – 19	Noise, propagation delay and power dissipation	**1**	
	12	17 – 01 – 19	17 – 01 – 19	Analysis and design of 2-I/P NAND using equivalent CMOS inverter	**1,4** **Video**	
	13	18 – 01 – 19	18 – 01 – 19	Analysis and design of 2-I/P NOR using equivalent CMOS inverter	**1,4**	
4	14	21 – 01 – 19	21 – 01 – 19	Problems	**1,4**	
	15	22 – 01 – 19	22 – 01 – 19	CMOS Latch up, Causes, Remedies		
	16	24 – 01 – 19	24 – 01 – 19	Static CMOS	1	Vide o
	17	25 – 01 – 19	25 – 01 – 19	**Project Based Learning**		
Assignment I				Submission on 29 – 02– 19		
Module 3 – MOS Circuit Design Styles						
5	18	28 – 01– 19	28 – 01– 19	Zipper, C_2MOS, sizing using logical effort design styles	**1,7**	
	19	29 – 01– 19	29 – 01– 19	Circuit Realization of SR Latch using Static CMOS Pseudo NMOS	**1,7**	
	20	01 – 02– 19	01 – 02– 19	Domino, NORA design styles , pass transistor logic, transmission gate design styles	**1,7**	
6	21	07 – 02– 19	07 – 02– 19	**Project Based Learning**	**1,7**	**Feb 4,5, 6 UT I**
	22	08 – 02– 19	08 – 02– 19	Circuit Realization of JK FF using Static CMOS	**1,7**	
7	23	11 – 02– 19	11 – 02– 19	1 Bit Shift Register using above design styles, Circuit Realization of D FF using Static CMOS		

	24	12 – 02– 19	12 – 02– 19	MUX, decoder using above design styles	**2,1,7**	
Module 4 - Data Path Design						
8	25	18 – 02– 19	18 – 02– 19	Bit adder circuits, ripple carry adder	**2,1,7**	
	26	21 – 02– 19	21 – 02– 19	CLA adder - Logic and Design	**2**	
	27	22 – 02– 19	22 – 02– 19	Multipliers - Partial-product generation	**2**	
s	28	25 – 02– 19	25 – 02– 19	partial-product accumulation, final addition, Booth's Algorithm	**2**	
	29	26 – 02– 19	26 – 02– 19	Multiplication using Recoding	**2**	
	30	28 – 02– 19	28 – 02– 19	**Project Based Learning**	**1,7**	
	31	01 – 03– 19	01 – 03– 19	Barrel shifter Logic and Design	**6,7**	
Module 5 – VLSI Clocking and System Design						
1 0	32	05 – 03– 19	05 – 03– 19	Various components of power dissipation in CMOS, Limits on low power design	**6**	
	33	07 – 03– 19	07 – 03– 19	CMOS clocking styles, Clock generation, stabilization and distribution	**6**	
	34	08 – 03– 19	08 – 03– 19	Low power design through voltage scaling	**6**	
				ESD protection, input circuits, output circuits,		
1 1	35	11 – 03– 19	11 – 03– 19	Simultaneous switching noise, power distribution scheme	**6**	
	36	12 – 03– 19	12 – 03– 19		**6**	
	37	14 – 03– 19	14 – 03– 19	**Project Based Learning**		
1 2	38	18 – 03– 19	18 – 03– 19	Interconnect delay model, interconnect scaling and crosstalk	**1,2,7**	
	39	19 – 03– 19	19 – 03– 19	Interconnect delay model, interconnect		

				scaling and crosstalk		
	40	22 – 03– 19	22 – 03– 19	ROM Array, SRAM operation, design strategy, leakage currents,		
Assignment II				Submission on 27 – 03 - 19		
Module6 – Semiconductor Memories						
13	41	25 – 03– 19	25 – 03– 19	Introduction to memory, 6T SRAM circuit, working & operation	**7**	
	42	26 – 03– 19	26 – 03– 19	SRAM operation, design strategy, leakage currents,	**7**	
	43	28 – 03– 19	28 – 03– 19	**Project Based Learning**		
	44	29 – 03– 19	29 – 03– 19	SRAM leakage currents, read/write circuits, sense amplifiers		
14	45	01 – 04– 19	01 – 04– 19	SRAM read/write circuits		
	46	02 – 04– 19	02 – 04– 19	DRAM - Operation 3T, 1T, operation modes, leakage currents		
	47	04 – 04– 19	04 – 04– 19	DRAM Refresh operation, Input-Output circuits		
	48	05 – 04– 19	05 – 04– 19	ROM Array, , NOR flash, NAND flash		
Total	**48**					

Recommended Books:

1. **Sung-Mo Kang and Yusuf Leblebici**, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition.
2. **Jan M. Rabaey,** Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.

3. **Etienne Sicard** and Sonia Delmas Bendhia, "*Basics of CMOS Cell Design*", Tata
   McGraw Hill, First Edition.
4. **Neil H. E. Weste,** David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. **Debaprasad Das**, "*VLSI Design*", Oxford, 1st Edition.
6. **Kaushik** Roy and Sharat C. Prasad, "*Low-Power CMOS VLSI Circuit Design*", Wiley, Student Edition.
7. **John P**. **Uyemura,** "Introduction to VLSI circuits and systems", Wiley student Edition

Practical Plan

CLASS	**TE Electronics, Semester VI**		
Academic Term	**Jan – Apl 2019**		
Subject	**VLSI Design (EXL603)**		

Evaluation System		***Hours***	***Marks***
	Practical Examination	--	--
	Oral Examination	--	25
	Term work	--	25
	Total	--	50

Time Table	***Day***	***Batch***	***Time***
	Monday	***C***	***11 – 1 pm***
	Tuesday	***D***	***11 – 1 pm***
	Wednesday	***A***	***11 – 1 pm***
	Thursday	***B***	***11 – 1 pm***

Title of Experiments

Sr. No.	***Title***	***Module***	***Attained POs***
1	Analysis of Input Output characteristics of NMOS & PMOS	Technology	PO1,

	transistor with **various model parameters.**	Trend	PO2,PO4
2	Comparative analysis of Voltage Transfer Characteristics of **Active and Passive load Inverters**.	MOSFET Inverter	PO1, PO2,PO4
3	**Static and Transient analysis of CMOS Inverter**.	MOSFET Inverter	PO1, PO2,PO4
4	Design and Implement **NAND/ NOR circuits** using various design styles (pseudo NMOS, dynamic CMOS, Domino etc.)	MOS Design Style	PO4
5	Implement the given equation y= (A.B+ C.D)' using **pass transistors.**	MOS Design Style	PO4
6	**Charge Sharing**.	MOS Design Style	PO1, PO2,PO4
7	Design and simulate **6 T SRAM**.	Semiconductor Memories	PO4
	Mini Project		PO1, PO2, PO3, PO9, PO10, PO12

Practical Session Plan

Batch	***Dates***		***Remarks***
	Planned	***Actual***	
Experiment No. 1 **Analysis of Input Output characteristics of NMOS & PMOS transistor with various model parameters .**			
C	14 – 01 – 19	14 – 01 – 19	
D	15 – 01 – 19	15 – 01 – 19	
A	16 – 01 – 19	16 – 01 – 19	
B	17 – 01 – 19	17 – 01 – 19	
Experiment No. 2 Comparative analysis of Voltage Transfer Characteristics of **Active and Passive load**			

Inverters .			
C	21 – 01 – 19	21 – 01 – 19	
D	22 – 01 – 19	22 – 01 – 19	
A	23 – 01 – 19	23 – 01 – 19	
B	24 – 01 – 19		Webinar by MHRD on 'Career, future industry trends and Startups'
Experiment No. 3 **Static and Transient analysis of CMOS Inverter**.			
C	28 – 01 – 19	28 – 01 – 19	
D	29 – 01 – 19	29 – 01 – 19	
A	30 – 02 – 19	30 – 02 – 19	
B	07 – 02 – 19	07 – 02 – 19	
Experiment No. 4 **Design and Implement NAND/ NOR circuits using various design styles (pseudo NMOS, dynamic CMOS, Domino etc.)**			
C	**11 – 02 – 19**	**11 – 02 – 19**	
D	**12 – 02 – 19**	**12 – 02 – 19**	**Feb 13-15 Euphoria**
A	**20 – 02 – 19**	**20 – 02 – 19**	
B	**21 – 02 – 19**	**21 – 02 – 19**	
Experiment No. 5 **Implement the given equation y= (A.B+ C.D)' using pass transistors.**			
C	18 – 02 – 19	18 – 02 – 19	
D	26 – 02 – 19	26 – 02 – 19	
A	27 – 02 – 19	27 – 02 – 19	
B	28 – 02 – 19	28 – 02 – 19	

Experiment No. 6 **Charge Sharing in circuit.**			
C	25 – 02 – 19	25 – 02 – 19	
D	05 – 03 – 19	05 – 03 – 19	
A	06 – 03 – 19	06 – 03 – 19	
B	07 – 03 – 19	07 – 03 – 19	
Experiment No. 7 Design and simulate **6 T SRAM .**			
C	11 – 03 – 19	11 – 03 – 19	
D	12 – 03 – 19	12 – 03 – 19	
A	13 – 03 – 19	13 – 03 – 19	
B	14 – 03 – 19	14 – 03 – 19	
8 **Mini Project – Approval, Basic Layout or block diagram**			
C	18 – 03 – 19	18 – 03 – 19	
D	19 – 03 – 19	19 – 03 – 19	
A	20 – 03 – 19	20 – 03 – 19	
B	28 – 03 – 19	28 – 03 – 19	
9 **Mini Project – Coding and Debugging**			
C	25 – 03 – 19	25 – 03 – 19	
D	26 – 03 – 19	26 – 03 – 19	
A	27 – 03 – 19	27 – 03 – 19	
B	04 – 04 – 19	04 – 04 – 19	
10 **Mini Project – Debugging and Verification, Report Submission**			
C	01 – 04 – 19	01 – 04 – 19	
D	02 – 04 – 19	02 – 04 – 19	

A	03 – 04 – 19	03 – 04 – 19	
B	04 – 04 – 19	04 – 04 – 19	

Term Work:

Term work assessment must be based on the **overall performance** of the student with **every experiment graded from time to time**. The grades should be converted into marks as per the **Credit and Grading System** manual and should be **added and averaged**. The grading and term work assessment should be done based on this scheme.

The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.

Laboratory work (Experiments and Journal) : 15 marks.

Test (at least one) : 10 marks.

Oral exam will be based on the entire syllabus.