Lesson Plan

Faculty: Sangeeta Parshionikar

CLASS		TE Electronics, Semester V	
Academic Term		July – Oct 2019	
Subject		**ASIC Verification (ELX DLO 5013)**	
Periods (Hours) per week	***Lecture***	***4***	
	Practical	***2***	
	Tutorial	***--***	
Evaluation System		***Hours***	***Marks***
	Theory examination	3	80
	Internal Assessment	--	20
	Practical Examination	--	--
	Oral Examination	--	25
	Term work	--	25
	Total	--	150

Time Table	***Day***	***Time***
	Monday	2.30 – 3.30 pm
	Tuesday	9.45 – 10.45 am
	Thursday	1.30 – 2.30 pm
	Friday	9.45 – 10.45 am

Course Content and Lesson plan

Module 1- Programmable Devices and Verilog

Week	Lecture No.	Date		Topic	Mapped CO	Mapped PO	References	Remarks (If any)
		Planned	Actual					
1	1	01 – 07 – 19	01 – 07 – 19	Introduction to ASIC Verification, Complete VLSI Flow(Frontend - Backend)	**CO1**	**PO1**	**1**	2nd to 7th July – STTP on IOT

	2	02 – 07 – 19	02 – 07 – 19	Architecture of FPGA, CPLD with an example of Virtex-7 and Spartan - 6 family devices	**CO1**	**PO1**	**1 Ref 4**	
	3	03 – 07 – 19	03 – 07 – 19	Data types, expressions, Design Hierarchy	**CO1**	**PO1**	**Ref Book 5 ,6**	
2	4	08 – 07 – 19	08 – 07 – 19	Gate and switch level modeling, Data flow modeling.	**CO1**	**PO1, PO3**	**Ref Book 5 ,6**	
	5	09 – 07 – 19	09 – 07 – 19	Behavioral modeling, Always and initial blocks, Blocking and non Blocking, delays, events, loops.	**CO1**	**PO1, PO3**	**Ref Book 5 ,6**	
	6	10 – 07 – 19	10 – 07 – 19	Example with all modelings,Tasks and functions.	**CO1**	**PO1, PO3**	**Ref Book 5 ,6**	
	Module 2 Verification Basics and Data Types							
3	7	15 – 07 – 19	15 – 07 – 19	Technology challenges, Verification methodology options, Verification methodology.	**CO1**	**PO1, PO2**	**1**	
	8	16 – 07 – 19		Testbench creation ,Verification Guidelines.	**CO1**	**PO1, PO2**	**1**	
	9	18 – 07 – 19		Testbench migration, Verification languages,Verification IP reuse, Verification approaches, Verification and device test.	**CO1**	**PO1, PO2**	**1**	
	10	19 – 07 – 19		Verification plans, reference design of Bluetooth SoC	**CO1**	**PO1, PO2**	**1, CH-2**	
4	11	22 – 07 – 19		Data Types**:** Built in, Fixed size array	**CO2**	**PO1, PO2**	**1, CH-2**	
	12	23 – 07 – 19		Dynamic array and methods	**CO2**	**PO1, PO2**	**1, CH-2**	

	13	25 – 07 – 19		Queue, associative array	**CO2**	**PO1, PO2**	**1, CH-2**	
	14	26 – 07 – 19		choosing a storage type,	**CO2**	**PO1**	**1, CH-3**	
5	15	29 – 07 – 19		Linked list, array methods, examples	**CO2**	**PO1**	**1, CH-3**	
	16	30 – 07 – 19		Type conversion, enumerated types	**CO2**	**PO1**	**1, CH-4**	
	18	01 – 08 – 19		creating new types with typedef, creating userdefined structures.	**CO2**	**PO1**	**1, CH-4**	
	18	02 – 08 – 19		Constants, Strings, expression width	**CO2**	**PO1**	**1, CH-4**	
Module 3-Procedural statements, test bench and Basic OOP								
6	19	05 – 08 – 19		Procedural statements, tasks, functions and void functions	**CO2**	**PO1**	**1, CH-4**	
	20	06 – 08 – 19		task and function overview, routine arguments, returning from a routine, local data storage, time values	**CO2**	**PO1, PO3**	**1, CH-4**	
	21	09 – 08 – 19		Separating the testbench and design, the interface construct, stimulus timing.	**CO3**	**PO1, PO3**	**1, CH-5**	
	22	19 – 08 – 19		Interface driving and sampling, connecting it all together, top level scope.	**CO3**	**PO1, PO3**	**1, CH-5**	
Unit Test I - 13th ,14th, 16th Aug 2019								
7	23	20 – 08 – 19		Class, Creating new objects, Object deallocation	**CO3**	**PO1, PO2**	**1, CH-5**	
	24	22 – 08 – 19		Object deallocation, using	**CO3**	**PO1,**	**1,**	

				objects, variables, class methods, defining methods outside class		**PO2**	**CH-5**	
	25	23 – 08 – 19		scoping rules, using one class inside another, understanding dynamic objects	**CO3**	**PO1, PO2**	**1, CH-6**	
8	26	26 – 08 – 19		Copying objects,	**CO3**	**PO1, PO2**	**1, CH-6**	
	27	27 – 08 – 19		public vs. local, building a testbench.	**CO3**	**PO1, PO2s**	**1, CH-6**	
	Module 4- Randomization and IPC							
8	28	29 – 08 – 19		Threads and Interprocess Communication	**CO3**	**PO1**	**1, CH-6**	
	29	30 – 08 – 19		working with threads, disabling and enabling threads	**CO3**	**PO1**	**1, CH-7**	
	30	09 – 09 – 19		Interprocess communication, Events, Semaphores	**CO3**	**PO1**	**1, CH-7**	
	31	12 – 09 – 19		IPC– Mailboxes, Semaphores, Events	**CO3**	**PO1**	**1, CH-7**	
	32	13 – 09 – 19		building a testbench with threads and IPC	**CO3**	**PO1**	**1, CH-8**	
9	33	16 – 09 – 19		Randomization in system Verilog, constraint details	**CO3**	**PO1**	**1, CH-8**	
	34	17 – 09 – 19		Solution Prabablities, Controlling multiple constraint blocks	**CO3**	**PO1**	**1, CH-8**	
	35	19 – 09 – 19		valid constraints, In-line constraints,	**CO3**	**PO1**	**1, CH-8**	
	36	20 – 09 – 19		The pre-randomize and post-randomize functions	**CO3**	**PO1**	**1, CH-9**	
10	37	23 – 09 – 19		Random number functions,	**CO3**	**PO1**	**1, CH-9**	
	38	24 – 09 – 19		Constraints tips and	**CO3**	**PO1**	**1,**	

				techniques, common randomization problems			**CH-9**	
	Module 5: Assertions and Functional Coverage							
	39	26 – 09 – 19		SystemVerilog Assertions in the Design Process, Formal Verification Using Assertions	CO3, CO4	**PO1, PO2**	**1, CH-9**	
	40	27 – 09 – 19		Understanding sequences and properties	CO3, CO4	**PO1, PO2**	**1, CH-9**	
11	41	30 – 09 – 19		Coverage types, strategies, Example	CO3, CO4	**PO1, PO2**	**1, CH-9**	
	42	01 – 10 – 19		examples, anatomy of a cover group	CO3, CO4	**PO1, PO2**		
	43	03 – 10 – 19		Triggering a cover group, data sampling,	CO3, CO4	**PO1, PO2**		
	44	03 – 10 – 19		Cross coverage, generic cover groups, Coverage options	CO3, CO4	**PO1, PO2**		
Total	**44**							
Unit Test II – 14th ,15th ,16th Oct 2019								

Text Books:

1. **Chris Spear**, "System Verilog for Verification: A guide to learning the testbench language features", Springer, 2nd Edition
2. **Stuart Sutherland, Simon Davidmann, and Peter Flake**, "System Verilog for Design: A guide to using system verilog for hardware design and modeling", Springer, 2nd Edition.

Reference Book:

1. **Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari and Lisa Piper**, "SystemVerilog Assertions Handbook", VhdlCohen Publishing, 3rd edition
2. **System Verilog Language Reference manual**
3. **S Prakash Rashinkar, Peter Paterson and Leena Singh**, "System on Chip Verification Methodologies and Techniques", Kluwer Academic, 1st Edition.
4. **Spartan and Virtex family user manuals from Xilinx**
5. **Verilog Language Reference manual**
6. **Samir Palnitkar, "**Verilog HDL: A guide to Digital Design and Synthesis" second edition,Pearson – IEEE 1364-2001 compliant.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.

• **Submitted By**	**Approved By**
Prof. Sangeeta Parshionikar	i) Prof. K. Narayanan Sign:
Sign:	ii) Prof. Sapna Prabhu Sign:
	iii) Prof. Shilpa Patil Sign:
	iv) Prof. Monica Khanore Sign:
Date of Submission: 15/07/19	**Date of Approval:**
Remarks by PAC (if any)	