

## Lesson Plan

*Faculty : Swapnali Makdey*

CLASS		BE Electronics Semester –VIII			
Academic Term		June 2019-Dec2019			
Subject		<b>IC Technology (ELXDL07034)</b>			
<i>Periods (Hours) per week</i>	<i>Lecture</i>	2			
	<i>Practical</i>	2			
	<i>Tutorial</i>	--			
<i>Evaluation System</i>		<i>Hours</i>	<i>Marks</i>		
	Theory examination	3	80		
	Internal Assessment		20		
	Practical Examination	--	--		
	Oral Examination	--			
	Term work	--			
	Total	--	100		
<b>Time Table</b>					
<i>Time Table</i>	<i>Day</i>	<i>Time</i>			
	Tuesday	8.45am – 9.45am			
	Wednesday	1.30pm to 2.30pm			
	Thursday	2.30pm to 3.30pm			
	Friday	9.45am – 10.45am			
<b>Course Content and Lesson plan</b>					
<i>(Also include dates of assignments, test paper and mention as remarks)</i>					
<b>Module 1: Environment and Crystal Growth for VLSI Technology</b>					
Week	Lecture No.	Date		Topic	Remarks(If any)
		Planned	Actual		
	1	2-7-2019		<b>1.1 Environment</b> : Semiconductor Technology trend	
	2	3-7-2019		Clean rooms, Wafer cleaning	
	3	4-7-2019		<b>1.2 Semiconductor Substrate:</b> Phase diagram and solid solubility,	

	4	8-7-2019		Cascode current mirrors and Active current mirrors	
	5	9-7-2019		Crystal structure, Crystal defects	
	6	10-7-2019		Czochralski growth, Float Zone growth	
	7	11-7-2019		Bridgman growth of GaAs	
	8	16-7-2019		Wafer Preparation and specification	
<b>Module 2: Fabrication Process Part 1</b>					
	9	18-7-2019		<b>2.1 Deposition:</b> Evaporation, Sputtering	
	10	19-7-2019		Chemical Vapor Deposition	
	11	23-7-2019		<b>2.2 Epitaxy:</b> Molecular Beam Epitaxy, Vapor Phase	
	12	24-7-2019		Epitaxy, Liquid Phase Epitaxy, Evaluation of epitaxial layers	
	13	25-7-2019		<b>Silicon Oxidation:</b> Thermal oxidation process	
	14	26-7-2019		Kinetics of growth, high $\kappa$ and low $\kappa$ dielectrics	
	15	29-7-2019		<b>Diffusion:</b> Nature of diffusion, Diffusion in a concentration gradient,	
	16	30-7-2019		Diffusion equation	
	17	31-7-2019		Impurity behavior, diffusion systems, evaluation of diffused layers Problems in diffusion,	
	18	1-8-2019		<b>Ion Implantation:</b> Penetration range, ion implantation systems	
	19	2-8-2019		Process considerations, implantation damage and annealing	
<b>Module 3 Fabrication Processes Part 2</b>					
	20	6-8-2019		<b>Etching :</b> Wet chemical etching, dry physical etching, dry chemical etching,	
	21	7-8-2019		reactive ion etching, ion beam techniques	
	22	8-8-2019		<b>Lithography:</b> Photoreactive materials, Pattern generation and mask making,	
	23	9-8-2019		pattern transfer, Electron beam, Ion beam and X-ray lithography	
	24	20-8-2019		<b>Device Isolation, Contacts and Metallization:</b> Junction and oxide isolation, LOCOS, trench isolation,	
	25	21-8-2019		Schottky contacts, Ohmic contacts,	

				Metallization and Packaging	
	26	22-8-2019		<b>CMOS Process Flow:</b> N well, P-well and Twin tub	
	27	23-8-2019		Design rules, Layout of MOS based circuits	
	28	27-8-2019		Buried and Butting Contact	
<b>Module 4 Measurements, Packaging and Testing</b>					
	29	28-8-2019		<b>Semiconductor Measurements:</b> Conductivity type, Resistivity, Hall Effect Measurements	
	30	29-8-2019		Drift Mobility, Minority Carrier Lifetime and diffusion length	
	31	30-8-2019		<b>Packaging:</b> Integrated circuit packages	
	<b>32</b>	11-9-2019		Electronics package reliability	
	33	11-9-2019		Testing: Technology trends affecting testing, VLSI testing process and test equipment	
<b>Module 5 SOI, GaAs and Bipolar Technologies</b>					
	34	11-9-2019		<b>SOI Technology:</b> SOI fabrication using SIMOX,	
	35	12-9-2019		Bonded SOI and Smart Cut	
	36	13-9-2019		PD SOI and FD SOI Device structure and their features	
	37	17-9-2019		<b>GaAs Technologies:</b> MESFET Technology,	
	38	18-9-2019		Digital Technologies, MMIC technologies, MODFET and Optoelectronic Devices	
	39	19-9-2019		<b>Silicon Bipolar Technologies:</b> Second order effects in bipolar transistor, Performance of BJT, Bipolar processes and BiCMOS	
<b>Novel Devices</b>					
	40	20-9-2019		<b>Multigate Device:</b> Various multigate device configurations (device structure and important features)	
	41	24-9-2019		<b>Nanowire:</b> Fabrication and applications	
	42	25-9-2019		<b>Graphene Device:</b> Carbon nanotube transistor fabrication, CNT applications	
	43	26-9-2019		FINFET Operation	
	44	27-9-2019		Video on IC fabrication	

	45	3-10-2019		Video on nano devices	
	46	4-10-2019		Discussion on university paper	

#### Recommended Books:

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, “*Silicon VLSI Technology*”, Pearson, Indian Edition.
2. Stephen A. Campbell, “*The Science and Engineering of Microelectronic Fabrication*”, Oxford University Press, 2nd Edition.
3. Sorab K. Gandhi, “*VLSI Fabrication Principles*”, Wiley, Student Edition.
4. G. S. May and S. M. Sze, “*Fundamentals of Semiconductor Fabrication*”, Wiley, First Edition.
5. Kerry Bernstein and N. J. Rohrer, “*SOI Circuit Design Concepts*”, Kluwer Academic Publishers, 1st edition.
6. Jean-Pierre Colinge, “*FinFETs and Other Multigate Transistors*”, Springer, 1st edition
7. M. S. Tyagi, “*Introduction to Semiconductor Materials and Devices*”, John Wiley and Sons, 1st edition.
8. James E. Morris and Krzysztof Iniewski, “*Nanoelectronic Device Applications Handbook*”, CRC Press
9. Glenn R. Blackwell, “*The electronic packaging*”, CRC Press
10. Michael L. Bushnell and Vishwani D. Agrawal, “*Essentials of Electronic Testing for digital, memory and mixed-signal VLSI circuits*”, Springer

#### Examination Scheme

Module		Lecture Hours	Marks distribution in Test (For internal assessment/TW)		Approximate Marks distribution in Sem. End Examination
			Test 1	Test 2	
1	Environment and Crystal Growth for VLSI Technology	08	05		20 marks
5	Fabrication Process Part I	10	05	04	20 marks
6	Fabrication Process Part II	10		06	8 marks

**Internal Assessment (IA):**

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered as final IA marks

**End Semester Examination:**

1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules