Lesson Plan

Faculty : Heenakausar Pendhari

CLASS	SE Electronics, Semester III			
Academic Term	July – Nov 2019			
Subject	**Digital Circuit Design (ELX 303)**			

Periods (Hours) per week	***Lecture***	***4***			
	Practical	***--***			
	Tutorial	***--***			
Evaluation System		***Hours***	***Marks***		
	Theory examination	3	80		
	Internal Assessment	--	20		
	Practical Examination	--	--		
	Oral Examination	--	--		
	Term work	--	--		
	Total	--	100		

Time Table	***Day***	***Time***		
	Monday	11am-12pm		
	Tuesday	9:45am-10:45am		
	Wednesday	1:30 pm – 2:30 pm		
	Friday	8.45am-9.45am		

Course Content and Lesson plan

Module 1 Number system and codes.

Week	Lecture No.	Date		Topic	References	CO	PO	Remarks (If any)
		Planned	Actual					
1	1	1 /7 / 19	1 /7 / 19	Discussion of syllabus and Cos of the subject, explain				

				students the importance of course out comes. Introduction to digital system.				
	2	2/7/19	1/7/19	Introduction to number system, binary, octal and hexadecimal, their conversion. Concept of basic gates AND, OR, Not, EX-or, symbol and truth table	Modern Digital Electronics, by R.P. Jain, Digital Design Morris Mano	ELX 303.1	PO1	Adjusted Prof. Archana's lecture
	3	3/7/19	3/7/19	Introduction to number system, binary, octal and hexadecimal, their conversion.		ELX 303.1	PO1	
	4	5/7/19	5/7/19	Binary Arithmetic: one's and two's complement		ELX 303.1	PO1	
	5	8/7/19	8/7/19	Binary Arithmetic: one's and two's complement		ELX 303.1	PO1	
	Module :2 Logic Gates and Boolean Algebra							
	6	9/7/19	09/7/19	Concept of basic gates AND, OR, Not, EX-or, symbol and truth table		ELX 303.1	PO1,PO3	
	7	10-7-19	10/07/19	Ex-nor, universal gates NAND, NOR their truth tables		ELX 303.1	PO1,PO3	
	8	12-7-19	10/7/19 (onleave therefore adjusted)	Boolean algebra, De-morgan's theorem, problems based on above rules.		ELX 303.2	PO1,PO3	
	9	15-7-19	15/7/19	Concept of SOP and POS , problems on SOP		ELX 303.2	PO1,PO3	
	10	16-7-19		Problems on POS, Minimization with		ELX 303.2	PO1,PO3	

				Karnaugh maps.				
	11	17-7-19		Problems on K-map, and realization of equations.		ELX 303.2	PO1,PO3	
	12	19-7-19		Quine-McClusky method upto four variables.		ELX 303.2	PO1,PO3	
	Module 3: Combinational Logic Circuits and Hazards.							
	13	22-7-19		Design of Half adder and Full adder using gates. Design of Half subtractor and Full Subtractor using gates.		ELX 303.3	PO1,PO3	
	14	23/7/19		Design of Half adder and Full adder using gates. Design of Half subtractor and Full Subtractor using gates.		ELX 303.3	PO1,PO3	
	15	24/7/19		Ripple carry adder , Carry Look ahead adder.		ELX 303.3	PO1,PO3	
	16	26/7/19		BCD adder, Magnitude comparator.		ELX 303.3	PO1,PO3	
	17	29/7/19		Designing multiplexer using gates, cascading of multiplexer		ELX 303.3	PO1,PO3	
	18	30/7/19		Designing de-multiplexer using gates, cascading of demultiplexer.		ELX 303.3	PO1,PO3	
	19	31/7/19		Boolean function implementation using multiplexer and gates.		ELX 303.3	PO1,PO3	
	20	2/8/19		Study of encoder and decoder		ELX 303.3	PO1,PO3	
	21	5/8/19		Parity Circuits, ALU		ELX 303.3	PO1,PO3	
		6/8/19		Assignment-1				
	22	6/8/19		Timing Hazards static and dynamic		ELX 303.2	PO1,PO3	
	23	7/8/19		Timing Hazards static and dynamic		ELX 303.2	PO1,PO3	

		Module 5: Sequential Logic Principles						
	24	9/8/19		Introduction to sequential circuits, Study of 1 bit memory cell, latches, concept of Flip-flop.	Digital Electronics, by R.P. Jain, Digital Design Morris Mano	ELX 303.3	PO1,PO2,PO3	
		13,15,16 AUG		**UNIT TEST-1**				
	25	19/8/19		S-R flip-flop, clocked S-R ff, D ff, T ff.		ELX 303.3	PO1,PO2,PO3	
	26,27	20/8/19,21/8/19		Jk ff, master salve JK ff. Conversion of flip flops Concept of registers.		ELX 303.3	PO1,PO2,PO3	
	28	23/8/19		Application of latches and flip flops in switch debouncing, bus holder circuits		ELX 303.3	PO1,PO2,PO3	
	29	26/8/19		Flip flops timing considerations and metastability		ELX 303.3	PO1,PO2,PO3	
		Module 6: Counters and Registers						
	30	27/8/19		Study of counters, Asynchronous counters designing using ffs.		ELX 303.3	PO1,PO2,PO3	
	31,32	28/8/19,30/8/19		Synchronous counters designing using ffs.		ELX 303.3	PO1,PO2,PO3	
		2nd-6th SEPTEMBER		**MID-TERM BEARK**				

	33,34	9/9/19,11/9/19		Designing UP Down counter		ELX 303.3	PO1,PO2,PO3	
	35,36	13/9/19,16/9/19		Mod counters using FFs, Ring counter.		ELX 303.3	PO1,PO2,PO3	
	37,38	17/9/19,18/9/19		Shift registers, SISO,SIPO. PISO, PIPO, universal shift register.		ELX 303.3	PO1,PO2,PO3	
		20/9/19	**ASSIGNMENT-2**					
	Module: 4. Logic Families							
	39	20/9/19		Study of logic family TTL , characteristics parameters.		ELX 303.4	PO1	
	40	23/9/19		Transfer characteristics of TTL NAND. Study of CMOS		ELX 303.4	PO1	
	41	24/9/19		Transfer characteristics of TTL NAND. Study of CMOS		ELX 303.4	PO1	
	42	25/9/19		Interfacing CMOS to TTL and TTL to CMOS		ELX 303.4	PO1	
	43	27/9/19		ECL working and characteristics		ELX 303.4	PO1	
	44	30/9/19		Discussion of university Question papers				

Text Books:

1. R. P. Jain, Modern Digital Electronics, Tata McGraw Hill Education, Third Edition 2003.
2. John F. Warkerly, Digital Design Principles and Practices, Pearson Education, Fourth Edition, 2008.

Reference Books:

1. A. Anand Kumar, Fundamentals of Digital Circuits, PHI, Fourth Edition, 2016.
2. Morris Mano / Michael D. Ciletti , Digital Design, Pearson Education, Fourth Edition, 2008.
3. Donald P. Leach / Albert Paul Malvino / Gautam Saha, Digital Principles and Applications, The McGraw Hill, Seventh Edition, 2011.

4. Thomas L. Floyd, Digital Fundamentals, Pearson Prentice Hall, Eleventh Global Edition, 2015.
5. Charles H. Roth, Fundamentals of Logic Design, Jaico Publishing House, First Edition, 2004.
6. Norman Balabanian/ Bradley Carlson, Digital Logic Design Principles, John Wiley & Sons, First Edition, 2011.

Examination Scheme

Module		Lecture Hours	Marks distribution in Test (For internal assessment/TW)		Approximate Marks distribution in Sem. End Examination
			Test 1	Test 2	
1	Number System and codes	6	5		15 marks
2	Logic Gates and Boolean Algebra	08	5		30 marks
3	Combinational Logic circuits and Hazards	12	10		30 marks
4	Logic Families	06		02	15 marks
5	Sequential Logic Principles	08		10	30marks
6	Counters and Registers	08		08	20 marks

Internal Assessment: (IA):
Two tests must be conducted which should cover atleast 80% of the syllabus. The average marks of both the test will be considered as final IA marks.

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. The students need to solve total 4 questions.
3. Question No. 1 will be compulsory and based on entire syllabus.
4. Remaining question (Q.2 to Q.6) will be set from all the modules.
5. Weightage of marks will be as per Blueprint.

Submitted By	**Approved By**
Prof. Heenakausar . Y. Pendhari	ii) Prof. K. Narayanan Sign:
Sign:	ii) Prof. Sapna Prabhu Sign:
	iii) Prof. Shilpa Patil Sign:
	iv) Prof. Monica Khanore Sign:
Date of Submission:15/7/19	**Date of Approval:**
Remarks by PAC (if any)	
