FR. Conceicao Rodrigues College Of Engineering

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

Department of Computer Engineering

S.E. (Computer) (semester III)

(2019-2020)

Course Outcomes & Assessment Plan

Subject: Digital Logic Design and Analysis (Course Code CSC302) Credits-4

Syllabus:

1. **Number Systems and Codes:**

Introduction to number system and conversions: Binary, Octal, Decimal and Hexadecimal number Systems, Binary arithmetic: addition, subtraction (1"s and 2"s complement), multiplication and division. Octal and Hexadecimal arithmetic: Addition and Subtraction (7"s and 8"s complement method for octal) and (15"s and 16"s complement method for Hexadecimal). Codes: Gray Code, BCD Code, Excess-3 code, ASCII Code. Error Detection and Correction: Hamming codes.

2. **Boolean algebra and Logic Gates**

Theorems and Properties of Boolean Algebra, Boolean functions, Boolean function reduction using Boolean laws, Canonical forms, Standard SOP and POS form. Basic Digital gates: NOT , AND , OR , NAND , NOR , EXOR , EX-NOR, positive and negative logic, K-map method 2 variable, 3 variable, 4 variable, Don"t care condition, Quine-McClusky Method, NAND-NOR Realization.

3. **Combinational Logic Design**

Introduction, Half and Full Adder, Half subtractor Full Subtractor, Four Bit Ripple adder, look ahead carry adder, 4 bit adder subtractor, one digit BCD Adder, Multiplexer, Multiplexer tree, Demultiplexer, Demultiplexer tree, Encoders Priority encoder, Decoders, One bit, Two bit , 4-bit Magnitude Comparator, ALU IC 74181.

4. **Sequential Logic Design**:

Introduction: SR latch, Concepts of Flip Flops: SR, D, J-K, T, Truth Tables and Excitation Tables of all types, Race around condition, Master Slave J-K Flip Flops, Timing Diagram, Flip-flop conversion, State machines, state diagrams, State table, concept of Moore and Mealy machine. Counters : Design of Asynchronous and Synchronous Counters,Modulus of the Counters, UP- DOWN counter, Shift Registers: SISO, SIPO, PIPO, PISO Bidirectional Shift Register, Universal Shift Register, Ring and twisted ring/Johnson Counter, sequence generator.

5. **Introduction to VHDL**

Introduction: Fundamental building blocks Library, Entity, Architecture, Modeling Styles, Concurrent and sequential statements, simple design examples for combinational circuits and sequential circuits

6. **Digital Logic Families**

Introduction: Terminologies like Propagation Delay, Power Consumption, Fan in and Fan out , current and voltage parameters, noise margin, with respect to TTL and CMOS Logic and their comparison

Course Objectives (optional):

1. To introduce the fundamental concepts and methods for design of digital circuits and a pre-requisite for computer organization and architecture, microprocessor systems.
2. To provide the concept of designing Combinational and sequential circuits.
3. To provide basic knowledge of how digital building blocks are described in VHDL.

Course Outcomes:

Upon completion of this course students will be able to:

CSC302.1: Perform number system and code conversions. (**Comprehension**)
CSC302.2: Design combinational circuits. (**Apply**)
CSC302.3: Design sequential circuits. (**Apply**)
CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design. **(Analyze , Apply)**

Mapping of CO and PO/PSO

Relationship of course outcomes with program outcomes: Indicate 1 (low importance), 2 (Moderate Importance) or 3 (High Importance) in respective mapping cell.

	PO1 (Engg Know)	PO2 (Ana)	PO3 (De sign)	PO4 (inve stiga)	PO5 (tools)	PO6 (engg Soci)	PO7 (Env)	PO8 (Eth)	PO9 (ind Team)	PO10 (com.)	PO11 (PM)	PO12 (life Long)
CSC302.1	3											
CSC302.2	3	2	3		1							
CSC302.3	3	2	3		1							
CSC302.4	3	3	3		3				2	2		
Course To PO	3	2.6	3		1.6				2	2		

CO	PSO1	PSO2
CSC302.1	3	
CSC302.2	3	
CSC302.3	3	
CSC302.4	3	
Course to PSO	3	

Justification

PO1: All COs are mapped to PO1 because engineering graduates will be able to apply the knowledge of **mathematics** & **Digital electronics fundamentals** to solve complex engineering problems.

Level 3 - The course demands mathematical concept to be applied to solve given problems. Also basic knowledge of digital electronics and fundamental of computer system is required.

PO2: CSC302.2, CSC302.3 and CSC302.4 are mapped to PO2 because the students **analyze** the given problem statement before designing the actual circuit.

Level 2 – CSC302.2 & CSC302.3 **Before designing any circuit for the given problem, students perform basic level of pre-analysis. (Analysis Includes identifying inputs - outputs, deriving truth table, minimization of output expression, Identify method for minimization, identify components to be used)**

Level 3 – CSC302.4 **– In order to provide a solution to a real world chosen problem, students design and then analyze the behavior of a circuit. Here students do rigorous analysis to obtain the desired output.**

PO3: CSC302.2, CSC302.3 and CSC302.4 are mapped to PO3 because the students **design** the digital circuits and implement them using hardware components.

Level 3: Because the course involves designing of various combinational and sequential circuits, students actually design the circuit and implement it in laboratory.

PO5:

CSC302.2 and CSC302.3 are mapped to PO5 because students use advance tool such as VHDL to analyze the basic combinational and sequential circuit.

Level 1 -Since basic analysis is done using VHDL.

CSC302.4 maps to PO5 because the students use various tools for example VHDL, Arduino Uno various actuators and sensors etc. to simulate/implement a real world problem.

Level 3 - Since students translate real world problem to digital network and analyze the circuit using various tools ; the nature of the problem is more complex here.

PO9: CSC302.4 is mapped to PO9 because the students work in a **team** to design and implement a solution for a chosen real world problem.
Level 2 - Since it's a mini project that give them first level of experience of being in a team; not rigorous team work is involved. Hence level is 2.

PO10: CSC302.4 is mapped to PO10 because the students explain mini project by demonstrating the project and also submit written report for the same.
Level 2 – basic level of presentation skills and written skills are expected.

PSO1: All COs are mapped to PSO1 because the graduates will be able to apply knowledge of Digital Electronics to simulate the real world problem.

Course Outcomes Target:

Upon completion of this course students will be able to:

CSC302.1: Perform number system and code conversions. (**Comprehension**)
CSC302.2: Design combinational circuits. (**Apply**)
CSC302.3: Design sequential circuits. (**Apply**)
CSC302.4: Simulate real world problems using VHDL**. (Analyze & Apply)**

Target:

CSC302.1: 2.5
CSC302.2: 2.5
CSC302.3: 2.5
CSC302.4: 2.5

Previous Years' Achievements

CO	Year 2018-19	Year 2017-18
CSC302.1	1.88	2.36
CSC302.2	2.2	2.2
CSC302.3	2.36	2.04
CSC302.4	3	2.44

CO Assessment Tools:

CSC302.1: Perform number system and code conversions

Direct Methods(80%): Test 1 + Module Test 1 + Quiz1 + UniExamTh + UniExam Pr

CO1dm = 0.2T1 + 0.2 MT+ 0.2 Q1 + 0.2UTh + 0.2 UPr

InDirect Methods(20%): Course exit survey

CO1idm

CSC302.1 = 0.8*CO1dm + 0.2* CO1idm

Direct Methods	Weightage	Target	Date	Marks
Test 1	0.2	**65%** students will score minimum 65% marks (i.6. 6 or more out of 10)		Q-1 (08M)
Module Test1	0.2	70% students will score minimum 70% marks (i.e. 7 or more out of 10)	4th week of July	10M
Quiz1	0.2	**65%** students will score minimum 70% marks (i.6. 14 or more out of 20)	4th week of July	20M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.2: Design combinational circuits.

Direct Methods(80%): (Test1+Test2) + Lab + Assignment1 + UniExamTh + UniExam Pr

CO2dm = 0.2T1 + 0.2Lab + 0.2A1 + 0.2UTh +0.2UPr

InDirect Methods(20%): Course exit survey

CO2idm

CSC302.2 = 0.8*CO2dm + 0.2* CO2idm

Direct Methods	Weightage	Target	Date	Marks
Test	0.2	60% students will score minimum 60% marks (i.6. score 9 or more out of 15)	T1-14/8/19	**18M** Q-2(8)+Q-3(4) in T1 & Q-1 (6M) T2
Lab	0.2	70% students will score minimum 70% marks.(i.e score 56 or more out of 80)	Exp 1 to 7 & Exp 11	80M
Assignment1	0.2	**70%** students will score minimum 70% marks (i.6. score 07 or more out of 10)		10M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.3: Design sequential circuits.

Direct Methods(80%): Test2 + Module Test 2 + Lab + UniExamTh + UniExamPr

CO3dm = 0.2T2 + 0.2M2 +0.2Lab + 0.2UTh + 0.2UPr

InDirect Methods(20%): Course exit survey

CO3idm

CSC302.3 = 0.8*CO3dm + 0.2* CO3idm

Direct Methods	Weightage	Target	Date	Marks
Test 2	0.2	60% students will score minimum 60% marks (i.6. score 9 or more out of 15)	T2- 15/10/19	14M [Q2(6) + Q3(8)] in T2
Lab	0.2	70% students will score minimum 70% marks.(i.e score 28 or more out of 40)	EXP 8,9,10 & 12	40M
Module Test 2	0.2	60% students will score minimum score 60% marks (i.e. score 12 or more out of 20)	1st week of October	20M
Uni Theory exam	0.2	60% students will score minimum 60% marks (i.6. 48 or more out of 80)		80M
Uni. Practical Exam	0.2	60% students will score minimum 70% marks (i.6. 17.5 or more out of 25)		25M

CSC302.4: Design and implement a solution for a simple real world problem based on the learned concepts of digital Logic design.

Direct Methods(80%): MiniProject , lab

CO4dm = 0.2 Lab + 0.8 MP

InDirect Methods(20%): Course exit survey

CO4idm

CSC302.4 = 0.8*CO4dm + 0.2* CO4idm

Direct Methods	Weightage	Target	Date	Marks
Lab	0.2	70% students will score minimum 70% marks.(i.e score 14 or more out of 20)	Exp. 3-12	100M
Mini Project	0.8	60% students will score minimum 70% marks.(i.e score 10.5 or more out of 15)	Submission: 1st and 2nd week of October	15M

Content Beyond Syllabus:

Introduction to IoT

Curriculum Gap:

Indicator	Poor	Average	Good	Excellent

- Introduction to 8085 Processor to get better and practical applications of registers and ALU.
- In order to understand current applications, trends and new directions in logic design following topics shall be covered.

Sr.No.	Curriculum gap contents	Action Plan
1	Introduction to IOT	Self-learning online resource is provided on Moodle and flip class room activity.

List of Experiments with CO mapping

Sr. No	Title	CO
1.	To study and verify the truth table of various logic gates using ICs and realize Boolean expressions using gates.	CSC302.2
2.	To realize basic gates using universal gates.	CSC302.2
3.	To realize arithmetic circuits i) Half adder ii) Full adder iii) Half subtractor iv) Full subtractor.	CSC302.2
4.	To realize binary to gray code and gray code to binary converter.	CSC302.2
5	To realize parity generator and detector.	CSC302.2
6.	To Study multiplexer IC and realization of full adder using multiplexer IC	CSC302.2
7.	To realize 2 bit magnitude comparator.	CSC302.2
8.	Study of flip-flops using IC's	CSC302.3
9.	To realize shift registers using flip flops	CSC302.3
10.	To realize asynchronous 3 bit up counter.	CSC302.3
11	To realize combinational circuit using VHDL	CSC302.2
12.	To realize basic Sequential circuit using VHDL	CSC302.3
13.	Mini Project – Design and Implement a real world problem using learned concepts of digital Electronics	CSC302.4

Timeline (2)	More than two session late (0)	Two sessions late (1)	One session late (1.5)	Early or on time (2)
Analysis of problem and Circuit optimization (2)	Failed to do proper analysis , Very complex circuit(0.5)	Analysis done. The circuit is structured but unnecessary lengthy (1.5)	N.A.	Detailed analysis done. The circuit is structured and efficient.(2)
Output (4)	Failed to implement a complete design. Partial implementation. No output (1)	Hardware implementation done but failed to show output due to some error. (2)	Hardware implementation done. Output shown but some of the test cases not working. (3)	Expected output shown. All test cases verified. (4)
PostLab Assignment (2)	Not able to solve(0)	Able to solve 25% (1)	Able to solve 50%(1.5)	Able to solve all questions(2)

Rubrics for Experiments:

Rubrics for the Mini Project:

Mini project that covers design and implementation of important Digital circuits' concepts of the course, is allotted to the students in groups. The requirements will be announced in advance and discussed in class. The students' progress on their project will be discussed in the practical session and faculty office. Finally at the time of submission the students will present the demonstration of their project in lab session and submit a report for the same.

Indicator	Poor	Average	Good	Excellent
Timeline Maintains project deadline (2)	More than two session late (0.5)	Two sessions late (1)	One session late (1.5)	Early or on time (2)
Completeness Complete all parts of project (3)	< 40% complete (1)	~ 60% complete (2)	~ 80% complete (2.5)	100% complete(3)
System Design (3) Block diagram And circuit realization	NA	Designed circuit with basic gates (2)	Designed with NAND or NOR but not minimum (2.5)	Correct Designed with NAND or NOR Logic (3)
Report Submission(2)	N/A	Submitted one session late (1)	Partial steps are followed (1.5)	All steps are followed and well documented (2)

Schedule of mini project submission:

Stages of mini project	Date of submission
Project topic submission	16-Sep-2019
Analysis submission	23-Sep-2019
Design Submission	30-Oct-2019
Implementation	Second week of October

Rubrics for Assignments:

Indicator	Very Poor	Poor	Average	Good	Excellent
Timeline (2)	Assignment not submitted (0)	More than one week late (0.5)	Two weeks late (1)	One week late (1.5)	Early or on time (2)
Organization (2)	N/A	Very poor readability and not structured (0.5)	Poor readability and somewhat structured (1)	Readable with one or two mistakes and structured (1.5)	Very well written and structured without any mistakes (2)
Solution (3)	N/A	All solutions incorrect (0)	More than 50% Solutions are incorrect (1)	20-30% solutions incorrect (2)	All problems solved correctly (3)
Depth and breadth discussion (3)	N/A	None in evidence; superficial at most (0.5)	Minor points/information may be missing and discussion is minimal (1)	Discussion centers on some of the points and covers them adequately (2)	Information is presented in depth and is accurate (3)

Assignments:

ASSIGNMENT 1:

Date of Assignment: 30-08-2019
Date of submission: 12-09-2019 Year: 2019-2020
Maps to CSC302.2: Design Combinational circuits

Real world problems:

Q-1 A step in space vehicle checkout depends on 4 sensors s1, s2, s3 and s4. Circuit is properly working if sensors s2 and at least two of the other three sensors are at logic 1. Implement the system.

Q-2 Design a circuit with 4 inputs that has outputs with a binary value equal to the number of inputs that are HIGH.

Q-3 Design a combinational logic circuit with a single output that will serve as an "auto buzzer circuit in a car. The circuit should output a HIGH signal (to sound a buzzer) for each of the following conditions:

1) A driver's DOOR is open and the KEYS are in the ignition.
2) If the SEAT is occupied and the SEATBELTS are not buckled and the KEYS are in the ignition.

Determine the truth table for the circuit described above. Determine the minimal circuit and draw it using NAND gates only.

[Hint: A – Door (1 - open , 0 - closed) , B – KEYS (1 – in ignition , 0 – Not in ignition), C – SEAT (1- occupied, 0 not occupied), D – SEAT BELT (1 – buckled, 0 – not buckled)]

Q-4 A bank wants to design an alarm system for its safety. The alarm will sound…..

1) If bank is open (B=1) and there is a robbery (R=1) , alarm at bank (BA=1) and police station (PA=1) will sound.
2) If bank is closed (B=0) and there is a robbery (R=1), alarm will sound at police station only (PA=1).
3) If there is a fire (F=1) while the bank is open (B=1) , the alarm will sound in the in the bank (BA=1) and fire station (FA=1).
4) If there is fire (F=1) while the bank is closed (B=0), alarm will sound at fire station (FA=1) only.

Determine the truth table and design the circuit using basic gates (AND, OR, NOT, EXOR etc).

Design problems:

Q-5 Design 4- bit BCD subtractor using 4-bit parallel adder (IC 7483).

Q-6 Design BCD to seven segment display decoder.

Q-7 Design a combinational logic circuit that will multiply two 2-bit numbers.

Q-8 Simplify using Quine's McCluskey method. $F(A,B,C,D) = \Sigma m(0,1,4,5,9,10,12,14,15) + \Sigma d\ (2,8,13)$.

Verify your answer using KAMP.

Q-9 Design **32:1 MUX** using **4:1 MUX**. How many MUX do you need?

Q-10 Design 24-bit magnitude comparator using IC 7485.

Q-11 Implement following Boolean function using 4:1 MUX. F(A,B,C,D,E) = Σm(0,1,2,3,6,8,9,10,13,15,17,20,24)

Module Test 1:

Class: S.E. Comp (Sem III) **Date: 26-07-2019**

Subject : DLDA **Time : 11:00 to 12:00**

Maps to CO1: Perform number system conversion

Set-1

Q-1 Convert decimal number 576.24 into Binary, ,octal, base 9 and Hexadecimal. [04]

Q-2 Construct Hamming code for 1010 using odd parity. [04]

Q-3 Convert (-89) into equivalent signed magnitude, 1'complement and 2'scomplement form [04]

Q-4 Perform subtraction using 2's complement. $(62)_{10} - (99)_{10}$ [04]

Q-5 Perform subtraction using 16's complement [04]

i) $(CB1)_{16} - (971)16$
ii) $(426)_{16} - DBA)_{16}$

Set -2

Q-1 Convert decimal number 1762.46 into Binary, octal , base 7 and Hexadecimal. [04]

Q-2 Construct Hamming code for 1010 using even parity. [04]

Q-3 Convert (-80) into equivalent signed magnitude, 1'complement and 2'scomplement form [04]

Q-4 Convert $(47.3)_{10}$ to Gray code [04]

Q-5 Perform Following [04]

i) addition of $(34)_8$ and $(62)_8$.
ii) Perform $(289)_H - (1AD)_H$ without converting to any other base.

Module Test 2:

Brach/ Semester: Computer/III — Date: 09-10-2019

Course: DLDA (CSC302) — Duration: 1 Hr.

Q-1 Implement following logic function using 8:1 Mux. [06]

$F(A,B,C,D) = \Sigma m(1,3,5,10,11,13,14)$

Q-2 Design Mod – 6 asynchronous counter. Also draw timing diagram. [07]

Q-3 Design MOD-6 synchronous counter using T flipflops. [07]

OR

Q-3 Design synchronous counter for the following sequence

0-> 1 -> 3 -> 4 -> 6 -> 0

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Department of Computer Engineering

S.E. (Computer) (semester III)

(2017-2018)

Lesson Plan : Digital Logic Design And Analysis

Semester III **Year: 2019-20**

Modes of Content Delivery:

i	Class Room Teaching	v	Self Learning Online Resources	Ix	Industry Visit
ii	Tutorial	vi	Slides	X	Group Discussion
iii	Remedial Coaching	vii	Simulations/Demonstrations	xi	Seminar
iv	Lab Experiment	viii	Expert Lecture	xii	Case Study

Lect. No.	Portion to be covered	Planned date	Actual date	Content Delivery Method/Learning Activities	Reference material
	MODULE 1: Number Systems and Codes				
1.	Introduction to the subject, Revision of Binary, Octal, Decimal and Hexadecimal number Systems.	**1/7/19**	**1/7/19**	Class Room Teaching	i
2	Number system conversion and Numerical on number system conversion	**3/7/19**	**3/7/19**	Class Room Teaching	i
3	Number system conversion and Numerical on number system conversion	**4/7/19**	**4/7/19**	Class Room Teaching	i
4	Binary Arithmetic: Binary Addition and Subtraction (1's complement and 2's complement)	**5/7/19**	**5/7/19**	Class Room Teaching	i
5	Multiplication & Division	**8/7/19**	**8/7/19**	Class Room Teaching	I
6	Octal and Hexadecimal arithmetic	**10/7/19**	**10/7/19**	Class Room Teaching	I
7	Codes: Gray, BCD, Excess 3 , ASCII Code	**11/7/19**	**11/7/19**	Class Room Teaching	I

8	Error Detection and correction codes: Hamming codes :	**12/7/19**	**12/7/19**	Class Room Teaching	i, iv
	MODULE 2:Boolean Algebra and Logic Gates				
9	Theorem and properties of Boolean algebra. Boolean functions and function reduction using Boolean laws.	**16/7/19**	**16/7/19**	Class Room Teaching	i
10	Canonical forms: SOP ,POS	**17/7/19**	**17/7/19**	Class Room Teaching	I,iv
11	Basic Digital gates: NOT , AND , OR , NAND , NOR , EXOR , EX-NOR, positive and negative logic. NAND-NOR Realization	**18/7/19 (cancelled due to talk)**	**19/7/19**	Class Room Teaching **[Video1]** **[TPS activity]**	i, iv
12	K-map method 2 variable, 3 variable, 4 variable, Don‟t care condition	**19/7/19**	**22/7/19**	Class Room Teaching	i, iv
13	K-map method 2 variable, 3 variable, 4 variable, Don‟t care condition.	**23/7/19**	**23/7/19**	Class Room Teaching	i, iv
14	Solving more problems using K-Maps and	**24/7/19**	**24/7/19**	Class Room Teaching **[TPS activity]**	i, iv
15	Quine-McClusky Method, NAND-NOR Realization.	**25/7/19**	**25/7/19**	Class Room Teaching	i, iv
16	Quine-McClusky Method Quine-McClusky Method. NAND-NOR Realization.	**26/7/19**	**25/7/19**	Class Room Teaching	i, iv
17	**Module Test1 -1**	**30/7/19**	**26/7/19**		
	Module 3: Combinational Logic Design				
18	Introduction to combinational logic, Half Adder , Full Adder	**31/7/19**	**30/7/19**	Class Room Teaching	i
19	Half Subtractor , Full subtractor	**1/8/19**	**31/7/19**	Class Room Teaching	i
20	Four Bit Ripple adder, look ahead carry adder, 4 bit adder subtractor	**2/8/19**	**2/8/19**	Class Room Teaching	I
21	Code converters : Binary to Gray, Gray to Binary, BCD to Binary, Binary to BCD	**6/8/19**	**6/8/19**	Class Room Teaching, Lab	i, iv

				Experiment	
22	Code converters: BCD to EX-3, EX-3 to BCD	**7/8/19**	**7/8/19**	Class Room Teaching	i, iv
23	One digit BCD Adder, One digit BCD Subtractor	**8/8/19**	**8/8/19**	Class Room Teaching	i
24	Encoders, Priority encoder, Decoders	**9/8/19**	**9/8/19**	Class Room Teaching	i, iv
25	Multiplexer, Multiplexer tree	**20/8/19**	**20/8/19**	Class Room Teaching, Lab Experiment	i, iv
26	Demultiplexer, Demultiplexer tree	**21/8/19**	**21/8/19**	Class Room Teaching	i, iv
27	One bit, Two bit, 4-bit Magnitude Comparator, ALU IC 74181.	**22/8/19**	**22/8/19**	Class Room Teaching, Lab Experiment	i, iv
	Module 4: Sequential Logic Design				
28	Introduction: SR latch , Concepts of Flip Flops: SR, D, J-K, T,	**23/8/19**	**23/8/19**	Class Room Teaching **[video2]**	I
29	Truth Tables and Excitation Tables of all types, Race around condition	**27/8/19**	**27/8/19**	Class Room Teaching, Lab Experiment	I
30	Master Slave J-K Flip Flops, Timing Diagram,	**28/8/19**	**28/8/19**	Class Room Teaching	I
31	Flip-flop conversion	**29/8/19**	**29/8/19**	Class Room Teaching	i, iv
32	Shift Registers: SISO, SIPO, PIPO, PISO	**30/8/19**	**1/9/19**	Class Room Teaching	i, iv
33	Bidirectional Shift Register	**11/9/19**	**13/9/19**	Class Room Teaching	i, iv
34	Universal Shift Register	**12/9/19**	**17/9/19**	Class Room Teaching, Lab	i, iv

				Experiment	
35	Ring and twisted ring/Johnson Counter	**13/9/19**	**18/9/19**	Class Room Teaching	i, iv
36	State machines, state diagrams, state tables. Concept of Moore and Mealy machine.	**17/9/19**	**18/9/19**	Class Room Teaching	i, iv
37	Counters: Design of Asynchronous Counters	**18/9/19**	**19/9/19**	Class Room Teaching, Lab Experiment **[Video3]**	i, iv
38	Counters: Design of Synchronous Counters	**19/9/19**	**20/9/19**	Class Room Teaching	i,iv
39	Modulus of the Counters	**20/9/19**	**24/9/19**	Class Room Teaching	i,iv
40	UP- DOWN counter	**24/9/19**	**25/9/19**	Class Room Teaching	i,iv
41	Sequence generator.	**25/9/19**	**26/9/19**	Class Room Teaching	i,iv
	Module 5: Introduction to VHDL				
42	Introduction: Fundamental building blocks Library, Entity	**26/9/19**	**3/10/19**	Class Room Teaching, **slides**	iii,v
43	Architecture, Modeling Styles	**27/9/19**	**3/10/19**	Class Room Teaching, **slides**	iii,v
44	Concurrent and sequential statements.	**30/9/19**	**4/10/19**	Class Room Teaching, **slides**	iii,v
45	simple design examples for combinational circuits, simple design examples for Sequential circuits.	**1/10/19**	**4/10/19**	Class Room Teaching, Lab Experiment	iii,v
	Module 6: Digital Logic Families				
46	Introduction: Terminologies like Propagation Delay, Power Consumption, Fan in and Fan	**3/10/19**	**9/10/19**	Class Room Teaching	I

	out , current and voltage parameters, noise margin,				
47	Comparison of TTL and CMOS Logic	**4/10/19**	**9/10/19**	Class Room Teaching	I
48	Flipped class room activity for ½ an hour and University Question papers Solution for ½ an hour	**5/10/19**	**11/10/19**	Class Room Teaching	

Resource	**Topic**	**Source**	**Type**
Video1	Transistors and Boolean logic	https://www.youtube.com/watch?v=SW2Bwc17_wA	You tube
Video2 Animation	RS Flip Flop	https://www.youtube.com/watch?v=--pv3MZMoo0	You tube
Video3	Introduction to counter	https://www.youtube.com/watch?v=iaIu5SYmWVM	You tube

Text Books/ Reference Books:

Te x t B o o k s :

Text Books:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. Yarbrough John M. , "Digital Logic Applications and Design ", Cengage Learning
3. J. Bhasker." VHDL Primer", Pearson Education

Reference Books:

4. M. Morris Mano, "Digital Logic and computer Design", PHI.
5. Douglas L. Perry, "VHDL Programming by Example", Tata McGraw Hill.
6. Donald p Leach, Albert Paul Malvino,"Digital principles and Applications", Tata McGraw Hill.

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Department of Computer Engineering

S.E. (Computer) (semester III)

(2019-2020)

LABORATOTY PLAN: DIGITAL SYSTEM LAB

Semester III **Year: 2019-20**

Sr. No	Title	CO	Planned dates	Actual dates			
	BATCH →			A	B	C	D
1.	To study and verify the truth table of various logic gates using ICs and realize Boolean expressions using gates.	CSC302.2	3rd week of July	17/7/19	16/7/19	15/7/19	15/7/19
2.	To realize basic gates using universal gates.	CSC302.2	4th week of July	24/7/19	23/7/19	22/7/19	22/7/19
3.	To realize arithmetic circuits i) Half adder ii) Full adder iii) Half subtractor iv) Full subtractor.	CSC302.2	1st week of August	31/7/19	30/7/19	29/7/19	29/7/19
4.	To realize binary to gray code and gray code to binary converter.	CSC302.2	2nd week of August	7/8/19	6/8/19	6/8/19	6/8/19
5	To realize parity generator and detector. (New)	CSC302.2	4th week of August	21/8/19	20/8/19	20/8/19	20/8/19
6.	To Study multiplexer IC and realization of full adder using multiplexer IC.	CSC302.2	1st week of September	28/8/19	27/8/19	27/8/19	27/8/19
7.	To realize 2 bit magnitude comparator.	CSC302.2	1st week of September	28/8/19	27/8/19	27/8/19	27/8/19
8.	Study of flip-flops using IC's	CSC302.3	2nd week of September	11/9/19	17/9/19	16/9/19	16/9/19
9.	To realize shift registers using flip flops	CSC302.3	2nd week of September	18/9/19	17/9/19	24/9/19	24/9/19
10.	To realize asynchronous 3 bit up counter.	CSC302.3	3rd week of September	25/9/19	24/10/19	30/9/19	30/9/19

11	To realize combinational circuit using VHDL	CSC302.2 CSC302.4	3rd week of September	9/10/19	1/10/19	7/10/19	7/10/19
12.	To realize basic Sequential circuit using VHDL	CSC302.3 CSC302.4	4th week of September	9/10/19	1/10/19	7/10/19	7/10/19
13.	Mini Project	CSC302.4		Submission 2nd week of October			