**Department of Information Technology**

**Course File Index**

**2018-19**

**Course Name: Computer Organization and Architecture** **Course ID:ITC404 Semester:IV**

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| Course Code | Course Name | Theory | Practical | Tutorial | Theory | Oral &  Practical | Tutorial | Total |
| ITC404 | Computer Organization and  Architecture | 04 | -- | -- | 04 | -- | -- | 04 |

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| Course Code | Course Name | Examination Scheme | | | | | | |
| Theory Marks | | | | Term Work | Oral & Practical | Total |
| Internal assessment | | | End Sem. Exam |
| Test1 | Test 2 | Avg. of two Tests |
| ITC404 | Computer Organizatio n and Architecture | 20 | 20 | 20 | 80 | -- | -- | 100 |

**Course Objectives:** Students will try to:

1. Conceptualize the basics of organizational and architectural issues of a digitalcomputer.
2. Analyze processor performance improvement using instruction levelparallelism.
3. Learn the function of each element of a memoryhierarchy.
4. Study various data transfer techniques in digitalcomputer.
5. Articulate design issues in the development of processor or other components that satisfy design requirements andobjectives.
6. Learn microprocessor architecture and study assembly languageprogramming.

**Course Outcomes:** Students will be able to:

1. Describe basic organization of computer and the architecture of 8086microprocessor.
2. Implement assembly language program for given task for 8086microprocessor.
3. Demonstrate control unit operations and conceptualize instruction levelparallelism.
4. Demonstrate and perform computer arithmetic operations on integer and realnumbers.
5. Categorize memory organization and explain the function of each element of a memory hierarchy.
6. Identify and compare different methods for computer I/Omechanisms.

**Prerequisite:** Fundamentals of Computer, Digital Logic Design

# Detailed syllabus:

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| --- | --- | --- | --- | --- |
| **Sr.**  **No.** | **Module** | **Detailed Content** | **Hours** | **CO**  **Mapping** |
| 0 | Prerequisite | basic combinational and sequential logic circuits, binary numbers and arithmetic, basic computerorganizations | 02 |  |
| I | Overview of Computer  Architecture & | Introduction of Computer Organization and Architecture. Basic organization ofcomputer  and block level description of thefunctional | 07 | CO1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Organization | units. Evolution of Computers, Von Neumann model. Performance measure of  Computer Architecture.  Architecture of 8086 family, 8086 Hardware Design, Minimum mode & Maximum mode of Operation. Study of bus controller 8288 & its use in Maximum mode. |  |  |
| II | Programming 8086 | Addressing modes, Instruction Set, Assembly Language Programming,Mixed  Language Programming, Programs based on Stacks, Strings, Procedures, Macros, Timers, Counters & delay. | 10 | CO2 |
| III | Processor Organization and  Architecture | CPU Architecture, Register Organization, Instruction formats, basic instruction cycle.  Instruction interpretation and sequencing.  Control Unit: Soft wired (Micro- programmed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming. Introduction to parallel processing concepts, Flynn’s classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards. | 11 | CO3 |
| IV | Data Representation and Arithmetic  Algorithms | Number representation: Binary Data representation, two’s complement  representation and Floating-point representation. Integer Data arithmetic: Addition, Subtraction. Multiplication: Unsigned & Signed multiplication- Add &Shift Method, Booth’s algorithm. Division of integers: Restoring and non-restoring division, signed division, basics of floating point representation IEEE 754 floating point(Single & double precision) number representation. Floating point arithmetic: Addition,subtraction | 10 | CO4 |
| V | Memory Organization | Introduction to Memory and Memory parameters. Classifications of primary and  secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associativememory. | 07 | CO5 |
| VI | I/O Organization | Input/output systems, I/O modules and 8089 IO processor. Types of data transfer  techniques: Programmed I/O, Interrupt driven I/O and DMA. | 05 | CO6 |

**Text Books:**

1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization”, Fifth Edition, Tata McGraw-Hill.
2. William Stallings, “Computer Organization and Architecture: Designing for Performance”, Eighth Edition,Pearson.
3. 8086/8088 family: Design Programming and Interfacing: By John Uffenbeck (PearsonEducation)
4. Microprocessor and Interfacing: By Douglas Hall (TMHPublication).

# References:

1. B. Govindarajulu, “Computer Architecture and Organization: Design Principles and Applications”, Second Edition, TataMcGraw-Hill.
2. Dr. M. Usha, T. S. Srikanth, “Computer System Architecture and Organization”, First Edition, Wiley-India.
3. John P. Hayes, “Computer Architecture and Organization”, McGraw-Hill.,ThirdEdition.
4. K Bhurchandi, “Advanced Microprocessors & Peripherals”, Tata McGraw-HillEducation

# Assessment:

**Internal Assessment for 20 marks:**

Consisting of **Two Compulsory Class Tests**

Approximately 40% to 50% of syllabus content must be covered in First test and remaining 40% to 50% of syllabus contents must be covered in second test.

**End Semester Examination:** Some guidelines for setting the question papers are as:

* + Weightage of each module in end semester examination is expected to be/will be proportional to number of respective lecture hours mentioned in thesyllabus.
  + Question paper will comprise of total **six questions**, **each carrying 20marks.**
  + **Q.1** will be **compulsory** and should **cover maximum contents of the syllabus**.
  + **Remaining question will be mixed in nature** (for example if Q.2 has part (a) from module 3 then part (b) will be from any other module. (Randomly selected from all themodules.)

Total **four questions** need to

**1.1 Course Outcome Statement**

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| --- | --- |
| **Sr.No.** | **Course Outcome Statement** |
| 1. | Describe basic organization of computer and the architecture of 8086 microprocessor. |
| 2. | Implement assembly language program for given task for 8086 microprocessor. |
| 3. | Demonstrate control unit operations and conceptualize instruction level parallelism. |
| 4. | Demonstrate and perform computer arithmetic operations on integer and real numbers. |
| 5. | Categorize memory organization and explain the function of each element of a memory hierarchy. |
| 6. | Identify and compare different methods for I/O mechanisms. |

**1.2 CO Assessment Tools**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Direct Methods** | | | | | | | | **Indirect Methods** |
|  | Test | Lab | University exam | quiz |  |  |  |  | Course Exit Survey |
| CO1 | 50% |  | 30% | 20% |  |  |  |  | 100% |
| CO2 |  | 80% | 20%(oral) |  |  |  |  |  | 100% |
| CO3 | 60% |  | 40% |  |  |  |  |  | 100% |
| CO4 | 60% |  | 40% |  |  |  |  |  | 100% |
| CO5 | 60% |  | 40% |  |  |  |  |  | 100% |
| CO6 | 60% |  | 40% |  |  |  |  |  | 100% |

**1.3 CO-PO and CO-PSO Mapping**

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| **Course Name** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 2 |  |  |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO2 |  |  | 3 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO3 |  |  | 1 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO4 | 1 |  | 2 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO5 | 1 |  |  |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO6 | 1 |  |  |  |  |  |  |  |  |  |  |  | 1 | 1 |
| LO1 | 2 |  |  |  |  |  |  |  |  |  |  |  | 1 | 1 |
| LO2 |  |  | 2 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| LO3 |  |  | 1 | 1 | 1 |  |  |  |  |  |  |  | 1 | 1 |
| LO4 |  |  | 1 | 1 | 1 |  |  |  |  |  |  |  | 1 | 1 |
| LO5 |  |  | 1 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| LO6 |  |  | 1 |  |  |  |  |  |  |  |  |  | 1 | 1 |

**1.4 Rubrics for assessment of Assignment:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Indicator** | **Poor** | **Average** | **Good** |
| Timeliness   * Maintains assignment deadline (3) | Assignment not done (0) | One or More than One week late (1-2) | Maintains deadline (3) |
| Completeness   * Complete all parts of assignment(3) | N/A | < 60% complete (1-2) | 60%-80% complete (2)  >80% complete (3) |
| Originality   * Extent of plagiarism(2) | Copied it from someone else(0) | At least one question has been copied(1) | Assignment has been solved completely by them self(2) |
| Knowledge   * In depth knowledge of the assignment(2) | Not able to answer any question (0) | Managed to answer 2 questions(1) | Able to answer all questions (2) |

**1.5 Rubrics for assessment of Experiment:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sr. No.** |  | **Exceed Expectation (EE)** | **Meet Expectation (ME)** | **Below Expectation (BE)** |
| 1. | On time submission  Or completion (2) | Early or on time (2) | One session late  (1) | More than one session late(0) |
| 2. | Preparedness(2) | Awareness about experiment to be performed, Knows the basic theory related to the experiment very well.(2) | Managed to explain the theory related to the experiment.  (1) | Not aware of the theory to the point.  (0) |
| 3. | Skill (4) | Structured and optimum performance  (4) | Few steps are not appropriate  (2) | Just managed  (1) |
| 4. | Documentation (2) | Lab experiment is documented in proper format and maintained neatly.  (2) | Most of the report is documented in proper format but some formatting guidelines are missed.  (1) | Experiments not written in proper format (0.5) |

**2.1 Lesson Plan**

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| **No of classes available:** | **43** | **No of Classes taken:** | **43** | |
|  |  |  |  | |
| **Sr. No.** | **Topic Planned** | **Planned Date** | **Actual Date** | **Delivery Mechanisms** |
| 1. | Overview of Computer organization & architecture | 1/1/19 | 1/1/19 | Blackboard&chalk |
| 2. | Programming 8086 | 11/1/19 | 11/1/19 | PPTs |
| 3. | Processor Organization & architecture | 24/2/19 | 24/2/19 | Blackboard&chalk |
| 4. | Data Representation and Arithmetic Algorithms | 16/2/19 | 16/2/19 | Blackboard&chalk |
| 5. | Memory Organization | 6/3/19 | 6/3/19 | Blackboard&chalk |
| 6. | I/o Organization | 27/3/19 | 10/4/19 | Blackboard&chalk |

**2.2 Date wise lecture plan**

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| --- | --- | --- | --- |
| Sr.no | Topics | Planned dates | Actual dates |
| 1. | Introduction to subject, Course outcomes, Syllabus for the subject | 2/1/19 | 2/1/19 |
| 2. | Need For studying COA, difference bet Computer Architecture,  Organization, blocks of computer system. | 3/1/19 | 3/1/19 |
| 3. | Revision of previous lect, Von-Nuemann machine, Stored program Concept | 7/1/19 | 7/1/19 |
| 4. | Brief description :address bus, databus,registers,8086 architecture, BIU, EU, Registers | 8/1/19 | 8/1/19 |
| 5. | Revision of previous lect Introduction to buses, Data ,Address, Control bus, System bus | 9/1/19 | 9/1/19 |
| 6. | Physical address calculation, instruction queue register, Addressing modes | 10/1/19 | 10/1/19 |
| 7. | Addressing modes continued, instruction set of 8086 | 11/1/19 | 11/1/19 |
| 8. | Types of 8086 instructions: data transfer, arithmetic instructions | 14/1/19 | 14/1/19 |
| 9. | Assembler Development Tools, assembly language programming | 15/1/19 | 15/1/19 |
| 10. | Assembler directives, programing in TASM | 17/1/19 | 17/1/19 |
| 11. | Surprise Test | 18/1/19 | 18/1/19 |
| 12. | Revision of previous lect Introduction to buses, Data ,Address, Control bus, System bus  Interconnection structures | 23/1/19 | 23/1/19 |
| 13. | Revision of previous lect Elements of Bus design, Function, Timing, mode of transfer,  Width, Multiple bus hierachy | 23/1/19 | 23/1/19 |
| 14. | Revision of previous lect Date representation, Types of representation for unsigned and  Signed numbers, Sign magnitude,1’s comp,2’s comp format, overflow  Advantages of 2’s comp representation, Adder and subtractorcircuits .  Serial Adder, Parallel Adder. | 24/1/19 | 24/1/19 |
| 15. | Revision of previous lect Disadvantages of parallel Adder, Fast Adder, Carry look ahead adder Multiplication, unsigned Multiplication algorithm, Example on unsigned multiplication , disadvantages. | 25/1/19 | 25/1/19 |
| 16. | Revision of previous lect Booth’s multiplication algorithm, examples, multiply 7\*-9,-14\*5,-18\*2,disadvantage,Bit pair recording  Advantage of Booth’s Multiplication. | 29/1/19 | 29/1/19 |
| 17. | Revision of previous lect Division, manual division, restoring division algorithm examples7/3 | 30/1/19 | 30/1/19 |
| 18. | Revision of previous lect Problem solving based on restoring division | 1/2/19 | 1/2/19 |
| 19. | Revision of previous lect Floating point representation, IEEE 754 representation, Biased exponent, significance of biased exponent | 7/2/19 | 7/2/19 |
| 20. | Revision of previous lect Conversion from one format to another, floating point ALU | 8/2/19 | 8/2/19 |
| 21. | Problems on IEEE floating point standards,conversion | 20/2/19 | 20/2/19 |
| 22. | Control unit design, generation of control signals | 21/2/19 | 21/2/19 |
| 23. | Single bus organization datapath in CPU. | 22/2/19 | 22/2/19 |
| 24. | Different contrl signals for instruction fetch operation, data operation | 26/2/19 | 26/2/19 |
| 25. | Horizontal and vertical microinstruction format,hardwired and microgrammed cu. | 27/2/19 | 27/2/19 |
| 26. | Surprise test | 28/2/19 | 28/2/19 |
|  | Control signals for complete excecution of instruction ADDR3,R1,Hardwire control unit block diagram | 1/3/19 | 1/3/19 |
| 27. | Revision of previous lect Memories: What is memory, Memory hierarchy, need of cache, locality of reference | 5/3/19 | 5/3/19 |
| 28. | Revision of previous lect Types of locality of reference:temporal and spatial,need of mapping techniques,types of mapping | 6/3/19 | 6/3/19 |
| 29. | Revision of previous lect Direct mapping and fully associative mapping with example, Disadvantages & advantages of direct mapping | 7/3/19 | 7/3/19 |
| 30. | Revision of previous lect Advantage and disadvantage of fully associative mapping,set associative mapping with example | 8/3/19 | 8/3/19 |
| 31. | Revision of previous lectComparsion of three mapping techniques, Need for replacement policies,FIFO,LRU | 12/3/19 | 12/3/19 |
| 32. | Revision of previous lect Problems on replacement policies, Elements of cache design multilevel,functions,typeswrite policies | 13/3/19 | 13/3/19 |
| 33. | Revision of previous lect Characteristics of two level memory wrtcost,size,speed,cache coherency | 14/3/19 | 14/3/19 |
| 34. | Revision of previous lect Solutions to problem of cache coherency,hardware and software solutions | 19/3/19 | 19/3/19 |
| 35. | Revision of previous lect Virtual memory concept,Translation of VA to PA with example, | 20/3/19 | 20/3/19 |
| 36 | Revision of previous lect Virtual memory contd , paging, MMU, need for TLB,Demand paging | 20/3/19 | 20/3/19 |
| 37. | Revision of previous lect Pipelining, need for pipelining,2 stage and 4 stage pipeline | 20/3/19 | 20/3/19 |
| 38. | Revision of previous lect Hazards in pipeline: data, structural, instruction controlwith example | 20/3/19 | 20/3/19 |
| 39. | Revision of previous lect Branch prediction logic,static dynamic solutions to control hazards. | 22/3/19 | 22/3/19 |
| 40. | Revision of previous lectComparision of sequential and pipelined execution,6 stage pipelining | 26/4/19 | 26/4/19 |
| 41. | Revision of previous lect | 28/3/19 | 28/3/19 |
| 42. | Revision of previous lect, I/O organization,Flynn’s classification, parallel processing | 29/3/19 | 29/3/19 |
| 43. | Guest Lecture |  |  |

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| Sr.no | Program Title | LO Mapping |  |
| 1. | A) To add two 8 bit numbers with carry | LO2,LO6 | Week 1 |
|  | B) To add two 16 bit numbers with carry | LO2,LO6 | Week 1 |
|  | C) To subtract two 8 bit numbers | LO2,LO6 | Week 1 |
| 2. | A) To multiply two 8 bit numbers | LO2,LO6 | Week 2 |
|  | B) To multiply two 16 bit numbers | LO2,LO6 | Week 2 |
|  | C) To divide two numbers. | LO2,LO6 | Week 2 |
| 3. | Program to move set of numbers from one memory block to another | LO3,LO6 | Week 3 |
| 4. | Program to count number of 1’s in a 8 bit number. | LO3,LO6 | Week 4 |
| 5. | Program to count even and odd numbers in set of 10 numbers. | LO3,LO6 | Week 5 |
| 6. | Program to find average of 10 numbers. | LO3,LO6 | Week6 |
| 7. | Program to arrange numbers in ascending order | LO3,LO6 | Week7 |
| 8. | Program to check whether a string is palindrome or not. | LO4,LO6 | Week 8 |
| 9. | Program to generate the first ‘n’ Fibonacci numbers. | LO4,LO6 | Week 9 |
| 10. | Study of Motherboard Components | LO1,LO6 | Week 10 |
| 11. | A) ADC Interfacing. | LO5,LO6 | Week 11 |
| 12. | B) DAC Interfacing. | LO5,LO6 | Week 11 |

Lab plan:

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