**FR. Conceicao Rodrigues College Of Engineering**

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

**Department of Information Technology**

**T.E. (IT) (Semester III)  (2019-2020)**

**Lesson Plan**

 **Subject: Logic Design(ITC302)**

 **Credits-4**

SYLLABUS

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| I |  Biasing of BJT | Biasing of BJT: DC operating point, BJT characteristics & parameters, all biasing circuits, analysis of above circuits and their design, variation of operation pointand its stability. DifferentialAmplifier, constant current source, current mirror. | 08 | CO1 |
| II | Number System and codes | Introduction to Number systems, Binary Number systems, SignedBinary Numbers, Binary, Octal, Decimal and Hexadecimal number Systems and their conversion, Binary arithmetic using compliments, Gray Code, BCD Code, Excess-3 code, ASCIICode.inter-conversion of codes, | 08 | CO2 |
| III | Boolean Algebraand Logic gates | Introduction, NAND and NORoperations, Exclusive –OR and Exclusive –NOR operations, Boolean Algebra Theorems and Properties , Standard SOP and POS form, Reduction of Boolean functions using Algebric method, K-map method (2,3,4 Variable).Variable entered Maps, Quine Mc Cluskey, Mixed Logic Combinational Circuits and multiple output functionBasic Digital Circuits: NOT,AND, OR,NAND,NOR,EX-OR,EX-NORGates. | 10 | CO2 CO3 |
| IV | Design and Analysis ofCombinational Circuits | Introduction, Half and Full Adder, Half and Full Subtractor, Four BitBinary Adder, One digit BCD Adder, code conversion, Encoder and Decoder ,Multiplexers and De- multiplexers, Decoders, Binary comparator (2,3 variable)4-bit Magnitude Comparator IC 7485 and ALU IC74181. | 08 | CO2CO3 CO4 |
| V | Sequential LogicDesign | Flip Flops : SR, JK, D, T, masterslave flip flop, Truth Table, excitation table and conversionRegister: Shift register, SISO, SIPO, PISO, PIPO, Bi-directional and universal shift register.Counters: Design of synchronous and asynchronous ,Modulo Counter, Up Down counter IC 74193, Ring and Johnson Counter | 9 | CO4CO5 |
| VI | VHDL | Introduction to VHDL, Library,Entity, Architecture Modeling styles, Concurrent and Sequential statements, data objects and datatypes, attributes, design examples | 07 | CO5CO6 |

Internal Assessment:

Internal Assessment consists of two tests. Test 1, an Institution level central test, is for 20 marks and is to be based on a minimum of 40% of the syllabus. Test 2 is also for 20 marks and is to be based on the remaining syllabus. Test 2 may be either a class test or assignment on live problems or course project.

**CO-Statements:**

CO1:Achieve Knowledge and Awareness of various components to design stable analog circuits.

CO2:Represent numbers and perform arithmetic operations.

CO3:Minimize the Boolean expression using Boolean algebra and design it using logic gates

CO4:Analyse and design combinational circuit.

CO5:Design and develop sequential circuits

CO6:Translate real world problems into digital logic formulations using VHDL.

**CO-PO-PSO Mapping**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course****Name** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO****11** | **PO****12** | **PSO1** | **PSO2** |
| CO1 | 2 |  | 2 |  |  |  |  |  |  |  |  |  | 1 | 1 |
| CO2 | 3 | 2 |  |  |  |  |  |  |  |  |  |  |  |  |
| CO3 | 3 | 2 | 2 |  |  |  |  |  |  |  |  |  |  |  |
| CO4 | 2 | 2 | 3 |  |  |  |  |  |  |  |  |  | 1 |  |
| CO5 | 2 | 2 | 3 |  |  |  |  |  |  |  |  |  | 1 |  |
| CO6 | 2 | 2 | 1 |  |  |  |  |  |  |  |  |  | 2 | 2 |

**CO Assessment Tools**

|  |  |  |
| --- | --- | --- |
|  | **Direct Methods** | **Indirect Methods** |
|  | **Test1** | **Assig1** | **Lab Work** | **Test2** | **Assig2** | **University Theory Exam** | **University Practical Exam** | Course Exit Survey |
| CO1 |  |  |  | **30%** | **25%** | **20%** | 25% | 100% |
| CO2 | **25%** | **30%** |  |  |  | **20%** | 25% | 100% |
| CO3 | **30%** | **15%** | 10% |  |  | **20%** | 25% | 100% |
| CO4 | **20%** | **10%** | **10%** |  | **15%** | **20%** | 25% | 100% |
| CO5 |  |  | **20%** | **20%** | **15%** | **20%** | 25% | 100% |
| CO6 |  |  | **25%** | **10%** | **20%** | **20%** | 25% | 100% |

**Lecture Plan:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No of classes available:** | **40** | **No of Classes taken:** | **42** |
|  |  |  |  |
| **Sr. No.** | **Topic Planned** | **Planned Date**  | **Actual Date** | **Delivery Mechanisms** |
| 1 | Prerequisites on semiconductor theory | 1/7/19 | 1/7/19 | Chalk and board |
| 2 | Introduction to number systems-Binary | 2/7/19 | 4/7/19 | Chalk and board |
| 3 | Octal Number system-Conversion | 4/7/19 | 5/7/19 | Chalk and board |
| 4 | Decimal number system-Conversion | 5/7/19 | 8/7/19 | Chalk and board |
| 5 | Hexadecimal number system-conversions | 8/7/19 | 9/7/19 | Chalk and board |
| 6 | Binary arithmetic using compliments | 9/7/19 | 11/7/19 | Chalk and board |
| 7 | Gray code, BCD | 11/7/19 | 12/7/19 | Chalk and board |
| 8 | Excess 3, ASCII, interconversion of codes | 12/7/19 | 15/7/19 | Chalk and board |
| 9 | Intoduction to Logic gates-Basic digital circuits | 15/7/19 | 17/7/19 | Chalk and board |
| 10 | NAND, Ex-or, EX-NOR operations | 17/7/19 | 18/7/19 | Chalk and board |
| 11 | Boolean algebra theorems and properties | 18/7/19 | 19/7/19 | Chalk and board |
| 12 | Standard SOP and POS form | 19/7/19 | 22/7/19 | Chalk and board |
| 13 | Reduction of Boolean functions using algebraic method | 22/7/19 | 23/7/19 | Chalk and board |
| 14 | K-map introduction | 24/7/19 | 24/7/19 | Chalk and board |
| 15 | Reduction using k-maps | 25/7/19 | 26/7/19 | Chalk and board |
| 16 | Quine McCluskey | 26/7/19 | 29/7/19 | Chalk and board |
| 17 | Mixed logic combinational circuits | 29/7/19 | 31/7/19 | Chalk and board |
| 18 | Half Adder, Full adder | 31/7/19 | 1/8/19 | Chalk and board |
| 19 | Half subtractor, full subtractor | 1/8/19 | 2/8/19 | Chalk and board |
| 20 | Four bit binary adder, one digit BCD adder | 2/8/19 | 7/8/19 | Chalk and board |
| 21 | Code conversion | 5/8/19 | 8/8/19 | Chalk and board |
| 22 | Encoder | 7/8/19 | 9/8/19 | Chalk and board |
| 23 | Decoder | 8/8/19 | 19/8/19 | Chalk and board |
| 24 | Multiplexer | 9/8/19 | 21/8/19 | Chalk and board |
| 25 | Demultiplexer | 19/8/19 | 22/8/19 | Chalk and board |
| 26 | Binary comparator | 21/8/19 | 23/8/19 | Chalk and board |
| 27 | Comparator using IC 7485 | 22/8/19 | 26/8/19 | Chalk and board |
| 28 | ALU IC 74181 | 23/8/19 | 28/8/19 | Chalk and board |
| 29 | Intro-sequential logic, Flip flops | 26/8/19 | 29/8/19 | Chalk and board |
| 30 | SR Flipflop, JK flipflop | 28/8/19 | 30/8/19 | Chalk and board |
| 31 | D, T Flipflop | 29/8/19 | 9/9/19 | Chalk and board |
| 32 | Master slave flipflop and conversion | 30/8/19 | 11/9/19 | Chalk and board |
| 33 | Register-shift register | 9/9/19 | 13/9/19 | Chalk and board |
| 34 | SISO, SIPO | 11/9/19 | 16/9/19 | Chalk and board, |
| 35 | PISO, PIPO | 13/9/19 | 18/9/19 | Chalk and board, |
| 36 | Bidirectional and universal shift register  | 16/9/19 | 19/9/19 | Chalk and board, |
| 37 | Counters-Design of synchronous and Asynchronous | 18/9/19 | 20/9/19 | Chalk and board |
| 38 | Modulo counterUp down counter, IC 74193 | 19/9/19 | 23/9/19 | Chalk and board |
| 39 | Ring and Johnson counter | 20/9/19 | 25/9/19 | Chalk and board, |
| 40 | Introduction to VHDL-Libraray | 23/9/19 | 26/9/19 | Chalk and board, |
| 41 | Entity, Architecture modeling styles | 25/9/19 | 27/9/19 | Chalk and board, |
| 42 | Concurrent and sequential satements | 26/9/19 | 28/9/19 | Chalk and board, |
| 43 | Data objects, Data types, Attributes | 27/9/19 | 28/9/19 | Chalk and board |
| 44 | Design examples for combinational circuits | 30/9/19 | 30/9/19 | Chalk and board, |
| 45 | Design examples for combinational circuits | 3/10/19 | 3/10/19 | Chalk and board |
| 45 | Introduction to BJT | 4/10/19 | 4/10/19 | Chalk and board |
| 46 | Biasing of BJT, Dc operating point | 7/10/19 | 7/10/19 | Chalk and board |
| 47 | BJT characteristics and parameters | 9/10/19 | 9/10/19 | Chalk and board |
| 48 | All biasing circuits | 10/10/19 | 10/10/19 | Chalk and board |
| 49 | Analysis of above circuits and their design | 11/10/19 | 11/10/19 | Chalk and board |
| 50 | Variation of operation point and its stability | 11/10/19 | 11/10/19 | Chalk and board |
| 51 | Differential amplifier | 17/10/19 | 17/10/19 | Chalk and board |
| 52 | Constant current source, current mirror | 17/10/19 | 17/10/19 | Chalk and board |

**Lab Plan for Digital Design Lab**

**Lab Outcomes:**

**Lab Outcomes:** Students will be able to:

LO1:Minimize the Boolean algebra and design it using logicgates.

LO2:Analyse and design combinationalcircuit.

LO3:Realise given function using combinationalcircuit.

LO4:Design and develop sequentialcircuits

LO5:Implement digital systems using programmable logicdevices

LO6:Translate real world problems into digital logic formulations usingVHDL.

Lab Plan:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sr.No. | **Module** | Detailed Content | **Hours** | **LO****Mapping** |
|  I | Boolean Algebra and Logic gates | 1. Verify the truth table oflogic

gates (basic and universal gates)1. Realization of Boolean algebra usinggates
 | 04 | LO1 |
| II | Design and Analysis ofCombinational Circuits | 1. Design of Full Adder andFull

Subtractor.1. Verify the operation of 4- bit magnitude comparator
 | 04 | LO2 |
| III | Implementation of CombinationalCircuits | 1. Implementation of MUXand

DeMUX.1. Implementation of Encoder and Decoder
 | 04 | LO3 |
| IV | Sequential Logic Design | 1. To verify and observethe

operation of flip-flop(any two)1. To design any two shiftregister.
2. To design Modulo andring Counter
 | 06 | LO4 |
| V | VHDL | 1. Implementation of Logic Gates usingVHD
2. Evaluate and observe combinational circuits on VHDL.
 | 04 | LO6 |

**Text Books:**

1. R. P. Jain, “Modern Digital Electronics”, Tata McGrawHill.
2. Balbaniam,Carison,”Digital Logic Design Principles”, WileyPublication

# References:

1. M. Morris Mano, “Digital Logic and computer Design”,PHI
2. J. Bhasker.“ VHDL Primer”, PearsonEducation.

# Term Work:

Term Work shall consist of at least 10 to 12 practical’s based on the above list. Also Term work Journal must include at least 2assignments.

**Term Work Marks:** 25 Marks (Total marks) = 15 Marks (Experiment) + 5 Marks (Assignments) + 5 Marks (Attendance)

**Oral & Practical Exam:** An Oral & Practical exam will be held based on the above syllabus

**Assignment Plan:**

|  |  |  |
| --- | --- | --- |
| **Assignment No** | **Date** | **CO** |
| **1** | **29/07/19** | **CO2,CO3,CO4** |
| **2** | **26/09/17** | **CO5** |
| **3** | **11/10/17** | **CO1** |

**Term Work:**

**Term Work:**

Term work Journal must include at least 2 assignments and Lab experiments.

**Term Work Marks:** 25 Marks (Total marks) = 15 Marks (Lab Experiments) + 5 Marks (Assignments) + 5 Marks (Attendance)