

Sangeeta Parshionikar

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A-42, "PARIJAT",
Bandra Reclamation,
Bandra (W), Mumbai – 400 050

Objective:

To achieve a challenging and rewarding position in the Educational Field where I can apply my engineering, analytical skills in the continuous process of learning and contributing for the development and expansion of the organization.

Synopsis:

- **16+ years** of experience **in Field of Education**
- **3 years** of Industry experience in **VLSI Design**

Education:

PhD(Computer Engineering, KL University, AP) - Pursuing

Mumbai University

Fr. Conceicao Rodrigues College of Engineering

ME in Electronics with distinction (75.56%)

Mar 2014

Nagpur University

Shri. Ramdeobaba Kamla Nehru Engineering College

BE in Electronics and Power Engineering (72.8%)

July 99

Other Professional Courses:

VLSI Design ('A' Grade)

Aug 02, CDAC Hyderabad

Diploma in Oracle 8.0 with Visual Basic 6.0

Apr 2000, SSI Nagpur

Achievements:

Received **Minor Research Grant** from University of Mumbai for the project "**Smart Air Pollution Monitoring system in Urban Environment**", 2017- 18.

Received **Minor Research Grant** from University of Mumbai for the project "**Stock Market Forecasting using Neural Network Implementation on FPGA**", 2018 -19.

Received **Minor Research Grant** from University of Mumbai for the project "**Smart Soil analyzer using IoT**", 2018 -19.

Team Member of "**Krushis Saurakshak**" project by leadindia.ai, a nation wide initiative By Bennette University, Greater Noida, India.

Received **appreciations** from the college for successfully coordinating the **workshops and FDPs**.

Delivered a **Lecture on "Introduction to VHDL and Its Scope"**, for an event conducted by WIE – IEEE, Fr. CRCE, Bandra.

Paper Published:

- A paper on **"Comparative Analysis of Deep Learning Techniques for Credit Card Fraud Detection"**, 2021 7th IEEE International Conference on Advances in Computing, Communication and Control, ICAC3 2021, and published in IEEE Xplore.
- A paper on **"A Chatbot as a First Responder for Panic Attack"**, IEEE Xplore, In press.
 - A paper on **"Skin Cancer Detection and Severity Prediction Using Computer Vision and Deep Learning"** is accepted and presented at Second International Conference on Sustainable Technologies for Computational Intelligence and under process of publication (expected in November 2021) in **Advances in Intelligent Systems and Computing** <https://www.springer.com/gp/book/9789811646409>
 - A paper on **"Verification of 32-bit Memory using Layered Testbench with Optimum Functional Coverage and Constrained Randomization"** published in Next Generation Information Processing System. **Advances in Intelligent Systems and Computing**, vol 1162. Springer, Singapore. https://doi.org/10.1007/978-981-15-4851-2_25.
 - A paper on **"Efficient Portable Camera Based Text to Speech Converter for Blind Person"**, presented at International Conference on Intelligent Sustainable Systems (ICISS), 2019. And published in **IEEE Xplore** . November 2019, **ISBN:978-1-5386-7800-8** DOI: [10.1109/ISS1.2019.8907995](https://doi.org/10.1109/ISS1.2019.8907995).
 - A paper on **"Generating hardware fingerprint of FPGA using physically Unclonable function"**, presented in International Conference on Recent Innovation in Electrical, Electronics and Communication Engineering, KIIT Bhubaneswar 27th & 28th July 2018.
 - A paper on **"Early detection of Heart disease using BRANN"** published in IJCRT Volume6, Issue 2, April 2018. DOI: <http://doi.org/10.1729/IJCRT.17983>
 - A Paper on **"Design and FPGA Implementation of High Speed UART"**, International Journal of Scientific and Engineering Research (**IJSER**) Volume 7, Issue 9, September 2016 Edition (ISSN 2229-5518) Pg no 106 - 110.
 - A paper on **"Design and analysis of 8x8 Static RAM"**, International Journal of Scientific and Engineering Research (**IJSER**) Volume 6, Issue 7, July 2015 Edition (ISSN 2229-5518) Pg no 338 - 342.
 - A paper on **"Leakage Power Reduction using Multi Threshold Voltage CMOS Technique"**, International Journal of Scientific and Engineering Research (**IJSER**) Volume 4, Issue10, October 2013 Edition (ISSN 2229-5518) Pg no 1077 - 1080.
 - A paper on **"Standby leakage power reduction techniques in Deep Sub micron CMOS VLSI circuits "**, **IJCA** and presented the same in International Conference on Communication Technology ICCT held in DJ Sanghvi College of Engineering, October 2013.

Responsibilities Handled:

Coordinator ISRO IIRS since August 2022

Convocation Coordinator for the year 2021, 2020, 2019, 2018, 2017.

B. E. Project coordinator for the department of Electronics since 2012.

IIC Social Media Coordinator for the year 2019- 20, 2020 - 21.

Coordinator – Syllabus Committee for the subject of ASIC Verification

Paper setter for various subjects of Mumbai University.

Reviewer for the ICAC3, International Conference at Fr. CRCE Bandra.

Reviewer for the IEEE-ICAST - 2022, K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai.

Reviewer for the CSCITA2023, International Conference at St. Francis Institute of Technology, Borivali, Mumbai

Hindi section Editor for College magazine FRAGMAG for the year 2010 – 2011.

Conducted workshop and FDPS.

Coordinator – Registration Committee - International Conference ICAC3'19 , ICAC3'21

FDPs & Workshops Conducted:

1. Two Week AICTE Sponsored Short Term Training Programme on "Research Areas in Technologies for Rural and Societal Development", December 21, 2020 - January 01, 2021.
2. One week FDP on "Advancements in IoT", 29 th May to 3 rd June 2020.
3. Two day workshop on ""Hands on FPGA applications", 23rd and 24th Feb., 2018
4. Two day workshop on" IC Technology:Layout to simulation" on September, 4th -5th , 2015.
5. Two day workshop on "Challenges in VLSI Design", 13 – 14 March, 2015.
6. Two day workshop on "Industrial Automation" on March 11th-12th ,2010

Professional Training:

- **NPTEL courses:**
 1. 8 weeks **NPTEL online course on "Introduction to Research" , Feb 2018 – April 2018**
 2. 8 weeks **NPTEL online course on "Enhancing Soft skill & Personality" , Feb 20, 2017 – April 14, 2017**
 3. 8 weeks **NPTEL online course on "Python for Data Science" , July - Aug, 2022. (75%)**
 4. 12 weeks **NPTEL online course on "Introduction to IOT", Jan - Apl 2020 (96%)**
 5. **ATAL AICTE Training and Learning academy FDP on "Deep Learning for NLP", 15/11/2021 to 19/11/2021.**

6. **ATAL AICTE Training and Learning academy FDP on “Object detection and Recognition using Deep Learning Techniques”**, 08/11/2021 to 12/11/2021
7. **Innovation Ambassador training** conducted by MoE’s Innovation cell and AICTE, 30th June - 30th July 2021.

• **STTP Courses :**

8. A one week FDP on “**ASIC Verification with System Verilog**”, at SPIT Andheri, Dec 21 -26.2015.
9. Attended ISTE approved one week STTP on “**Accreditation & Quality Assurance, Outcome based Education**”, at Fr. CRCE, Bandra, Nov 17 – 21, 2014.
10. Attended AICTE sponsored National level STTP on “**VLSI and Embedded Systems**” at Fr. CRIT Vashi, July 01 - 05, 2013.
11. One week ISTE STTP on “**Tools and techniques for effective technical writing**” at K.J. Somaiya College of Engg. Vidyavihar, May 13 -17, 2013.
12. A two week graded STTP on “**Basics Electronics**” conducted by **IIT, Bombay**, July 2011.
13. A one week STTP on “**Image Processing Applications :Basics to Advanced**” at St. Francis Institute of Technology, January 2010.
9. A one week STTP on “**Electromagnetic Waves and Its Applications**”, at SPIT June 2009
10. A Two week STTP on “**Robotics and its Applications**”, at Fr. CRCE, Dec. 2007.

Teaching Experience:

- 1). **Assistant Professor, Fr. Conceicao Rodrigues College Of Engineering, Bandra**
 July 2007 – Till Date
 Subjects: Internet of Things, Basic VLSI Design, ASIC Verification, Basic Electrical and Electronic Engineering, Computer Organization, Digital system design
- 2). **Lecturer, Shri. Ramdeobaba Kamla Nehru Engineering College, Nagpur**
 Jul 01, 00 to May 31, 01
 Subjects: Electrical Technology and Instrumentation, Digital Design
- 3). **Lecturer, Lady Anusayabai Daga College, Nagpur.**
 Sept 3, 99 to June 30, 00
 Subjects: Electrical Engineering and Network Theory

VLSI Design Industry Experience:

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| ❖ Name of Organisation | : PowaiLabs Pvt. Ltd., Mumbai. |
| Designation | : Product Testing Team Lead |
| Duration | : 1 st Mar’2006 – June’ 2007 |
| ❖ Name of Organisation | : Taray Technology Pvt. Ltd., Hyderabad. |
| Designation | : Design Engineer |
| Duration | : 13 th Sep’2005 – 13 th Dec’2005 |
| ❖ Name of Organisation | : STRATeL Microsystems Pvt. Ltd., Delhi. |
| Designation | : Member of Technical Team |
| Duration | : 1 st June’2004 – 31 th Aug’2005 |

Other Software Skills:

Language : Python, HSpice, VHDL, System Verilog, Verilog, C – programming,
Oracle, VB 6.0
Packages : MS Office 2000, MS Visio
Operating Systems : Windows, Linux, MS-DOS

Personal Information:

Date of Birth : 17th April 1978
Marital Status : Married
Languages : English, Hindi, Marathi
Personal Interest : Music, Meditation, Yoga, Reading