**n Course Outcomes & Assessment Plan**

**S.E. (Electronics and Computer Science) (semester III)**

**Subject: *Digital Electronics (ECC303)* Academic Term: *July –December 2022***

***Faculty name : Shilpa Patil***

**Syllabus:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Module No.** | | **Unit No** | | **Contents** | | | | **Hrs.** | |
| **1** | |  | | **Fundamentals of Digital Design** | | | | 07 | |
|  | 1.1 | **Number Systems and Codes:** Review of Number System, Binary Code, Binary Coded | | |  |
|  | | Decimal, Octal Code, Hexadecimal Code and their conversions, Binary Arithmetic: One's  and two's complements, | | | |
| 1.2 | | **Codes:** Excess-3 Code, Gray Code, Weighted code, Parity Code: Hamming Code | | | |
| 1.3 | | **Logic Gates and Boolean Algebra:** Digital logic gates, Realization using NAND, NOR gates, Boolean Algebra, De Morgan’s Theorem, SOP and POS representation, K Map up to four variables | | | |  | |
|  | **2** |  | | **Combinational Circuits using basic gates as well as MSI devices** | | | | 07 |  |
|  | | 2.1 | | **Arithmetic Circuits:** Half adder, Full adder, Ripple carry adder, Carry Look ahead adder, Half Subtractor, Full Subtractor, multiplexer, cascading of Multiplexer, demultiplexer,  decoder, Comparator (Multiplexer and demultiplexer gate level upto 4:1). | | | |  | |
| 2.2 | | **MSI devices:** IC7483, IC74151, IC74138, IC7485. | | | |
| **3** | |  | |  | **Elements of Sequential Logic Design** | | | 07 |  |
| 3.1 | | **Sequential Logic:** Latches and Flip-Flops. RS, JK, Master slave flip flops, T & D flip flops with various triggering methods, Conversion of flip flops, | | | |  | |
| 3.2 | | **Counters:** Asynchronous, Synchronous Counters, Up Down Counters, Mod | |  | |
| Counters, Ring Counter, Twisted ring counter, Shift Registers, Universal Shift Register. | | | |
| **4** | |  | |  | **Sequential Logic Design:** | | | 07 |  |
| 4.1 | | **Sequential Logic Design:** Mealy and Moore Machines, Clocked synchronous state machine analysis, State reduction techniques (inspection, partition and implication chart method) and state assignment, sequence detector, Clocked synchronous state machine design. | | | |  | |
| 4.2 | | **Sequential logic design practices:** MSI counters (7490, 7492, 7493,74163, 74169) and applications, MSI Shift registers (74194) and their applications. | | | |
| **5** | |  | | **Logic Families and Programmable Logic Devices** | | | | 05 | |
| 5.1 | | **Logic Families:** Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND(Operation of TTL NAND gate),CMOS Logic:CMOS inverter, CMOS NAND and CMOS NOR, Interfacing CMOS to TTL and TTL to CMOS. | | | |
| 5.2 | | **Programmable Logic Devices**: Concepts of PAL and PLA. Simple logic implementation using PAL and PLA, Introduction to CPLD and FPGA architectures, Numericals based on PLA and PAL | | | |  | |
| **6** | |  | | **Introduction to Verilog HDL** | | | | 06 | |
| 6.1 | | **Basics**: Introduction to Hardware Description Language and its core features, synthesis in digital design, logic value system, data types, constants, parameters, wires and registers.  **Verilog Constructs:** Continuous & procedural assignment statements, logical, arithmetic,  relational, shift operator, always, if, case, loop statements, Gate level modelling, Module instantiation statements. | | | |
| 6.2 | | **Modelling Examples:** Combinational logic eg. Arithmetic circuits, Multiplexer, Demultiplexer, decoder, Sequential logic eg. flip flop, counters. | | | |
|  | | **Total** | | | | **39** | |

**Course Outcomes:**

**After successful completion of the course, students will be able to:**

**ECC303.CO1.** Perform code conversion and binary arithmetic.

**ECC303.CO2.** Apply Boolean algebra and K-Map for the minimization of logic functions.

**ECC303.CO3.** Analyze and design Combinational and Sequential logic circuits using gates, flipflops as well as MSI chips.

**ECC303.CO4.** Distinguish between TTL & CMOS logic families w.r.t. their characteristic parameters and will be able to interface the ICs of the two families.

**ECC303.CO5.** Describe the structure of PLDs, CPLD and FPGA and the concepts of digital design with programmable devices.

**ECC303.CO6.** Illustrate the use of HDL (Verilog) for designing Digital circuits.

**Relationship of course outcomes with program outcomes:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **PO1** | **PO2** | **PO3** | **PO5** | **PSO1** |
| **ECC303.CO1** | 3 |  |  |  |  |
| **ECC303.CO2** | 3 |  |  |  |  |
| **ECC303.CO3** | 3 | 2 | 3 |  |  |
| **ECC303.CO4** | 3 |  |  |  |  |
| **ECC303.CO5** | 3 |  | 2 |  | 1 |
| **ECC303.CO6** | 3 |  | 2 | 2 | 1 |
| **Course mapping** | 3 | 2 | 2.3 | 2 | 1 |

**Justification of CO to PO mapping**

|  |  |  |
| --- | --- | --- |
| **CO1** | **PO1** | Acquire the knowledge of different number systems, codes and code conversions. |
| **CO2** | **PO1** | Learn about the logic function minimization and realization using the basic building blocks. |
| **CO3** | **PO1** | Acquire the knowledge of various MSI devices used in digital circuits. |
| **PO2** | Analyze the operation of a finite state machine. |
| **PO3** | Students can design simple combinational and sequential circuits systems using the the MSI devices. They also learn to design the finite state machine using basic building blocks. |
| **PO9** | Students study digital design for few simple real life applications and present in front of the class in the form of ppt or charts. They work in groups of 4 students each.  This activity involves team work and presentation skills. |
| **PO10** |
| **CO4** | **PO1** | Students learn about the logic families, their basic circuits, characteristics and understand the concept of compatibility and interfacing. |
| **CO5** | **PO1** | Acquire the knowledge of PLDs, CPLD, FPGA structure. |
| **PO3** | Students understand the concepts of designing with programmable devices. |
| **CO6** | **PO1** | Students learn the basics of the HDL Verilog |
| **PO3** | Students learn to write HDL code for digital design with reconfigurable devices. |
| **PO5** | Students learn to write Verilog codes as tool to design digital systems by using CPLD, FPGA |

**Justification of CO to PSO mapping**

|  |  |  |
| --- | --- | --- |
| **CO5** | **PSO1** | Students understand the use of reconfigurable digital devices in embedded systems which they can use in their projects. |
| **CO6** | **PSO1** | Students learn the basics of Verilog programming for reconfigurable devices which they can use in embedded system projects. |

[***To read POs and PSOs click here***](http://www.frcrce.ac.in/index.php/crce-department/elex-compsci/peo-po-elex-compsci)

**CO Assessment Tools:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| ***Course Outcome*** | ***Assessment Method*** | | | | | |
| ***Direct Method (80 %)*** | | | | | ***Indirect Method (20%)*** |
| Unit Tests | | Quiz (On each topic) | Assignment | End sem. Exam. | Course exit survey |
| UT1 | UT2 |  |  |  |  |
| CO1 | 25% |  | 25% |  | 50% | 100% |
| CO2 | 25% |  | 25% |  | 50% | 100% |
| CO3 | 15% | 15% | 10% | 10% | 50% | 100% |
| CO4 |  | 25% | 25% |  | 50% | 100% |
| CO5 |  | 20% | 10% | 20% | 50% | 100% |
| CO6 |  | 20% | 20% | 10% | 50% | 100% |

**CO calculation= (0.8 \*Direct method + 0.2\*Indirect method)**

**Rubrics for Assignment Grading:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Indicator** | **0** | **1** | **2** | **3** | **4** |
| Timeline (1) | Late submission | On time | — | --- | --- |
| Neatness(1) | Shabbily written | Neatly written | — | --- | --- |
| Level of content (4) | --- | 25% questions correctly answered with adequate steps/description | 50% questions correctly answered with adequate steps/description | 75% questions correctly answered with adequate steps/description | All questions correctly answered with adequate steps/description |
| Reading and Understanding (4) | --- | No understanding | Superficial  understanding | Understood to large extent | Well understood concepts and related topics |

**Curriculum Gap identified: (with action plan)**

No curriculum gap

**Content beyond syllabus:**

* Some design examples beyond syllabus will be discussed in the class.
* A guest lecture on “Industrial applications of FPGA”

**Modes of delivery:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Modes of Delivery** | **Brief description of content delivered** | **Attained COs** | **Attained POs** |
| Classroom teaching using board, PPTs, lectures | All Modules will be covered through classroom teaching which will include blackboard teaching, use of PPTs, videos, activities like think-pair- share, flipped classroom | CO1,CO2,CO3, CO4, CO5, CO6 | PO1,PO2,PO3 |
| Videos | Unit 6 will be partially covered through videos. | CO2, CO3, CO4 | PO1 |
| Guest lecture | An industry expert’s lecture on applications of CPLD, FPGA | CO1, CO5 | PO1, PSO1 |

**Reference Books:**

| **Sr. No.** | **Authors, Title and Publisher of the book** |
| --- | --- |
| Ref. 1 | R. P. Jain, Modern Digital Electronics, Tata McGraw Hill Education, Third Edition 2003 |
| Ref. 2 | Morris Mano, Digital Design, Pearson Education, Asia 2002 |
| Ref. 3 | Digital Logic Applications and Design – John M. Yarbrough, Thomson Publications, 2006 |
| Ref. 4 | John F. Warkerly, Digital Design Principles and Practices, Pearson Education, Fourth Edition, 2008 |
| Ref. 5 | Stephen Brown and ZvonkoVranesic, Fundamentals of digital logic design with Verilog design, McGraw Hill, 3rd Edition |
| Ref. 6 | Verilog HDL by Sameer Palnitkar, Pearson |
| Ref. 7 | J. Bhaskar, A Verilog HDL Primer  Third Edition, Star Galaxy Publishing, 2018 |

**Lesson Plan**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Class:*** | | | | | | **SE Electronics and Computer Science, Semester III** | | | | | |  |
| ***Academic Term :*** | | | | | | **July-December 2022** | | | | | |  |
| ***Subject:*** | | | | | | **Digital Electronics (ECC303)** | | | | | |  |
| ***Periods (Hours) per week*** | | | **Lecture** | | | | 3 hours | | | | |  |
| **Practical** | | | | 2 hours | | | | |  |
| ***Evaluation System*** | | |  | | | | ***Hours*** | ***Marks*** | | | |  |
| **Theory examination** | | | | 3 | 80 | | | |  |
| **Internal Assessment** | | | | -- | 20 | | | |  |
| **Practical Examination** | | | | -- | 25 | | | |  |
| **Term work** | | | | -- | 25 | | | |  |
| **Total** | | | | -- | 100 | | | |  |
| ***Time Table*** | | | ***Day*** | | | | ***Time*** | | | | |  |
| Tuesday | | | | 1.30 pm to 2.30 pm | | | | |  |
| Thursday | | | | 09.45 am to 10.45 pm | | | | |  |
| Friday | | | | 11.00 am to 12.00 | | | | |  |
| ***Course Content and Lesson plan*** | | | | | | | | | | | |  |
| **Week** | **Sr. No.** | **Date** | | | **Topic** | | | | **Refer-ences** | **Mapped** | | **Remark** |
| **Planned** | | **Actual** |  | | | | **CO** | **PO** |  |
| ***Module 1: Fundamentals of Digital Design*** | | | | | | | | | | | |  |
| 1 | 1 | 25-07-2022 | | 25-07-2022 | Introduction to the course  Number Systems and Codes: Review of Number System, Binary Code, Binary Coded Decimal, Octal Code, Hexadecimal Code and their conversions, Binary Arithmetic: One's and two's complements | | | | Ref. 1, 2 | CO1 | PO1 | MCQ1 based on number systems |
| 2 | 26-07-2022 | | 26-07-2022 | Codes: Excess-3 Code, Gray Code, Weighted code, Parity Code: Hamming Code | | | | CO1 |
| 3 | 28-07-2022 | | 27-07-2022 | Logic Gates and Boolean Algebra: Digital logic gates, Realization of logic function using gates | | | | CO2 | MCQ2 based on Boolean Algebra and logic gates |
| 2 | 4 | 01-08-2022 | | 01-08-2022 | NAND, NOR gates, Boolean Algebra, De Morgan’s Theorem, Function minimization using Boolean Algebra | | | | CO2  CO2 |
| 5 | 02-08-2022 | | 02-08-2022 | SOP and POS representation, K Map | | | | Ref. 1, 2 | PO1 |
| 6 | 04-08-2022 | | 04-08-2022 | Examples of function minimization and implementation using K Map | | | | Self Feedback |
|  | **Module 2: Combinational Circuits using basic gates as well as MSI devices** | | | | | | | | | | | |
| 3 | 7 | 11-08-2022 | | 11-08-2022 | Half adder, Full adder, Ripple carry adder, Half Subtractor, Full Subtractor | | | | Ref. 1, 2 | CO3 | PO, PO3 | Assignment1 based Combibnati-onal circuit design |
| 8 | 12-08-2022 | | 12-08-2022 | Carry Look ahead adder, IC7483 | | | |
| 4 | 9 | 18-08-2022 | | 18-08-2022 | Multiplexer, cascading of Multiplexer, IC74151 | | | |
| 10 | 19-08-2022 declared holiday | | 23-08-2022 | Demultiplexer, decoder, IC74138 | | | |
| 5 | 11 | 23-08-2022 | | 25-08-2022 | Comparator, IC7485 | | | |
| 12 | 25-08-2022 | | 26-08-2022 | Design examples with MSI devices | | | |
| 13 | 26-08-2022 | | 30-08-2022 | Design examples with MSI devices | | | |
|  | **Module 3: Elements of Sequential Logic Design** | | | | | | | | | | | |
| 6 | 14 | 30-08-2022 | | 08-09-2022 | Latches and Flip-Flops. RS, JK, Master slave flip flops, T & D flip flops | | | |  | CO3 | PO1 | 1. MCQ3 based on combinational MSI chips and Flipflops  2. Self Feedback |
| **Term Break from 31st August to 4th September**  **Unit Test 1 from 5th to 7th September 2022** | | | | | | | | |  |  |  |  |
| 7 | 15 | 08-09-2022 | | 09-09-2022 | Characteristic equations, Conversion of flip flops, | | | |  | CO3 | PO1 |  |
| 16 | 09-09-2022 | | 13-09-2022 | Asynchronous, Synchronous  Counters, | | | | Ref.1, 2, 3 | CO3 |  |  |
| 8 | 17 | 13-09-2022 | | 15-09-2022 | Up Down Counters, Mod n  Counters | | | |  |
| 18 | 15-09-2022 | | 16-09-2022 | Shift Registers, Universal Shift  Register | | | |  |
| 19 | 16-09-2022 | | 20-09-2022 | Ring Counter, Twisted ring  counter, applications | | | | Flipped classroom |
| **Module 4: Sequential Logic Design** | | | | | | | | | | | |  |
| 9 | 20 | 20-09-2022 | | 22-09-2022 | Mealy and Moore Machines, Clocked synchronous state machine analysis | | | | Ref. 3, 4 | CO3 | PO2, PO3 | Assignment2 based Sequential circuit design |
| 21 | 22-09-2022 | | 23-09-2022 | State reduction techniques (inspection, partition and implication chart method) | | | |
| 22 | 23-09-2022 | | 27-09-2022 | state assignment, example of sequence detector design | | | |
| 10 | 23 | 27-09-2022 | | 29-09-2022 | Clocked synchronous state machine design. | | | | Ref. 1, 3 |
| 24 | 29-09-2022 | | 30-09-2022 | MSI counters (7490, 7492, 7493,74163, 74169) and Shift registers (74194) | | | |
| 25 | 30-09-2022 | | 04-10-2022 | Designing with MSI counters and shift registers | | | |
| **Module 6: Introduction to Verilog HDL** | | | | | | | | | | | |  |
|  |  | Self Study with the help of Videos | | Basics: Introduction to HDL and its core features, synthesis in digital design, logic value system, data types, constants, parameters, wires and registers. Verilog Constructs: Continuous & procedural assignment,  Logical, arithmetic, relational, shift operator, always, if, case, loop statements, Gate level modeling, Module instantiation statements | | | | | Ref. 6, 7 | CO6 | PO1, PO3, PO5 | MCQ 4 based on Verilog |
| 11 | 26 | 04-10-2022 | | 06-10-2022 | Modeling Examples:Arithmetic circuits | | | |
| 27 | 06-10-2022 | | 07-10-2022 | Multiplexer, Demultiplexer, decoder, | | | |
| 28 | 07-10-2022 | | 11-10-2022 | Sequential logic eg. flip flop, counters, registers | | | |
|
|  | **Module 5: Logic Families and Programmable Logic Devices** | | | | | | | | | | | |
| 12 | 29 | 11-10-2022 | | 13-10-2022 | Introduction to logic family, Characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in) | | | | Ref. 1, 2 | CO4 | PO1 | MCQ3 based on logic families |
| 30 | 13-10-2022 | | 14-10-2022 | TTL NAND circuit operation, transfer characteristics of TTL NAND, Operation of TTL NAND gate | | | |
| 31 | 14-10-2022 | | 20-10-2022 | CMOS inverter, CMOS NAND and CMOS NOR, Interfacing CMOS to TTL and TTL to CMOS, Comparison of CMOS,TTL. | | | |
| **Unit Test 2 (from 17th to 19th October 2022)** | | | | | | | | | |  |  |  |
| 13 | 32 | 20-10-2022 | | 21-10-2022 | Concepts of PAL and PLA. Simple logic implementation using PAL and PLA, | | | | Ref. 4, 5 | CO5 | PO1 | Assignment3 based on function implementation with PLD and on Verilog coding |
| 33 | 21-10-2022 | | 27-10-2022 | Design examples based on PLA and PAL | | | | PO3 |
| **Diwali Holidays** | | | | | | | | |  |
| 14 | 34 | 27-10-2022 | | 28-10-2022 | Introduction to CPLD | | | | PO1 |
| 35 | 28-10-2022 | | Shared a video | Introduction to FPGA architectures | | | | Guest lecture on CPLD/FPGA |
| **Term End on 30th October 2022** | | | | | | | | | | | | |

**Examination Scheme:**

| **Module** | | **Lecture Hours** | **Marks distribution in Test** | | |
| --- | --- | --- | --- | --- | --- |
| **Test 1** | **Test 2** | **End Sem.Exam. (Approximate)** |
| 1 | Fundamentals of Digital Design | 7 | 8 | 0 | 20 |
| 2 | Combinational Circuits using basic gates as well as MSI devices | 7 | 8 | 0 | 20 |
| 3 | Elements of Sequential Logic Design | 7 | 4 | 4 | 20 |
| 4 | Sequential Logic Design: | 7 | 0 | 8 | 20 |
| 5 | Logic Families and Programmable Logic Devices | 5 | 0 | 7 | 20 |
| 6 | Introduction to Verilog HDL | 6 | 0 | 5 | 20 |

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| --- | --- |
| **Submitted By :** Shilpa J. Patil | **Approved By :**  Dr. D.V. Bhoir |
| **Sign:** | **Sign:Sd/-** |
| **Date of Submission: 08/08/2022** | **Date of Approval: 08/08/2022** |
| **Remarks by PAC member : Very Nicely and neatly done, Few real life applications will help students implement concepts and go beyond syllabus.** | |