FR. Conceicao Rodrigues College Of Engineering

Father Agnel Ashram, Bandstand, Bandra-west, Mumbai-50

Department of Electronics Engineering

Lecture Plan:

Subject: DIGITAL SYSTEMS DESIGN (DSD-ELX404) Credits-4

S.E. (ELECTRONICS) (semester IV) (2018-2019)

1. SYLLABUS

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ELX404	Digital System Design	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Oral &Practical	Total
		Internal assessment			End Sem. Exam			
		Test1	Test 2	Avg.				
ELX404	Digital System Design	20	20	20	80	--	--	100

Module No.	Topics	Hrs.
1	**Sequential logic design** Mealy and Moore models, state machine notations, clocked synchronous state machine analysis, construction of state diagram, sequence detector (word problem), state reduction techniques (inspection, partition and implication chart method), clocked synchronous state machine design, design examples like a few simple machines and traffic light controller, vending machine.	09
	Algorithmic State Machine (ASM) Chart and Register Transfer Luanguage(RTL)	

2	Standard symbols for ASM Chart, Realization techniques for sequential/logic functions using ASM Chart, Top Down Design Example, Generalized ASM output, ASM Chart representation of control unit, RTL, Construction of data unit using RTL Description, Timing of connection and transfer, sequencing of control, Combinational logic and conditional transfer, Graphical and RTL Bus notation, Design examples of waveform controllable generator ,pulse width adjustor using ASM chart, design data unit and control unit for sequential circuits using RTL Description.	**08**
3	**Sequential logic design practices** Synchronous counter design and applications, MSI asynchronous counters (IC 7490, 7493), MSI synchronous counters (IC 74161, 74163, 74168, 74169) and applications, decoding binary counter states, MSI shift registers, Synchronous design methodology, impediments in synchronous design, synchronizer failure and metastability.	**09**
4	**Introduction to VHDL** Introduction to Hardware Description Language, Core features of VHDL, data types, concurrent and sequential statements, data flow, behavioral, structural architectures, subprograms, Examples like Adder, subtractor, Multiplexers, De-multiplexers, encoder, decoder.	**08**
5	**Design of Sequential circuits using VHDL** VHDL code for flip flop, counters, registers, Moore, Mealy type FSMs, Serial adders, sequence detector.	**08**
6	**Programmable Logic Devices** ROM, RAM, SRAM, PLA, PAL, CPLD and FPGA architecture. Numerical based on PLA and PAL.	**06**
	Total	**48**

2. Course Outcomes:

At the end of the course student will be able to

ELX 404.1: Analyze various synchronous sequential logic circuits.

ELX 404.2: Design and implement synchronous sequential logic circuits.

ELX 404.3: Develop simple digital circuits using VHDLand verify using FPGA .

ELX 404.4 : Explain various applications of FPGAs in digital circuits.

ELX 404.5: Create a technical document of the design project and present ideas effectively.

3. Mapping of CO with PO/PSO:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
ELX 404.1	3	2											1	
ELX 404.2	3		2										2	
ELX 404.3	3		2		2								2	
ELX 404.4	2				2									
ELX 404.5	3		3		2			2	3	3		2		
	3	2	3		2			2	3	3		2	2	

4.CO Assessment Tool

Course Outcome						***Assessment Method***		
						Direct Method (80 %)		***Indirect Method (20%)***
	Unit Tests		Assignments		Laboratory Practical	University Results		Course exit survey
	1	2	1	2		Theory	Practical/ Orals	
ELX 404.1	20 %		10%		20%	30%	20%	100%
ELX 404.2	20 %		10%		20%	30%	20%	100%
ELX 404.3		10 %		20%	20%	30%	20%	100%

ELX 404.4				10%	40%	30%	20%	100%
ELX 404.5					50%		50%	100%

5. Curriculum Gap/Content beyond syllabus (if any).

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6. Lecture Plan.

6. Lecture Plan.

CLASS		**SE Electronics, Semester IV**			
Academic Term		**Jan – May 2019**			
Subject		**Digital System Design (ELX 404)**			
Periods (Hours) per week	***Lecture***	***4***			
	Practical	***--***			
	Tutorial	***--***			
Evaluation System		***Hours***	***Marks***		
	Theory examination	3	80		
	Internal Assessment	--	20		
	Practical Examination	--	--		
	Oral Examination	--	--		
	Term work	--	--		
	Total	--	100		
Time Table	***Day***	***Time***			
	Monday	1:30 pm – 2:30 pm			
	Tuesday	3:30 pm – 4:30 pm			
	Wednesday	12:00 pm – 1:00 pm			
	Thursday	11:00 am – 12:00 pm			

Course Content and Lesson plan								
Module 1 Sequential Logic Design								
Week	**Lecture No.**	**Date**		**Topic**	**Text Book-TB** **Reference Book-RB**	**CO**	**PO**	**Remarks (If any)**
		Planned	**Actual**					
1	1	7 /1 / 19	7 /1 / 19	Discussion of syllabus and Cos of the subject, explain students the importance of course out comes. Revision of digital circuits.	**TB-2**			
	2	8/1/19	8/1/19	Introduction to sequential state machines, classification: Mealy and Moore machine block diagram examples.	TB-1,2	ELX 404.1	PO1	
	3	9/1/19	9/1/19	Examples on analysis of Sequential circuit mealy machines	TB-1,2	ELX 404.1	PO1, PO2	
	4	10/1/19	10/1/19	Examples on analysis of Sequential circuit mealy machines, moore machine	TB-1,2	ELX 404.1	PO1, PO2	
	5	14/1/19	14/1/18	Examples on analysis of Sequential circuit moore machine	TB-1,2	ELX 404.1	PO1, PO2	
	6	15/1/19	15/1/19	Sequence detector examples	TB-1,RB-1	ELX 404.2	PO1, PO3	

	7	17/1/19	17/1/19	Sequence detector examples	TB-1,RB-1	ELX 404.2	PO1, PO3	
	8	18/1/19	18/1/19	Sequence detector examples	TB-1,RB-1	ELX 404.2	PO1, PO3	
	9	21/1/19	21/1/19	State reduction techniques	TB-1	ELX 404.2	PO1, PO3	
	10	22/1/19	22/1/19	State reduction techniques	TB-1	ELX 404.2	PO1, PO3	
	11	24/1/19	24/1/19	Traffic light controller : Examples	TB-1	ELX 404.2	PO1, PO3	
	12	25/1/19	25/1/19	Vending machine: Examples	TB-1	ELX 404.2	PO1, PO3	
	Module 3 Sequential logic design practices							
	13	19/3/19	18/3/19	Synchronous counter design and applications 74161, 74163	TB-2	ELX 404.2	PO1, PO3	
	14	22/3/19	19/3/19	Synchronous counter design and applications 74168, 74169	TB-2	ELX 404.2	PO1, PO3	
	15	25/3/19	20/3/19	Asynchronous counter design and applications 7490,7493	TB-2	ELX 404.2	PO1, PO3	
	16	26/3/19	25/3/19	Synchronous design methodology, Synchronizer failure and metastability	TB-2	ELX 404.2	PO1, PO3	

	17	28/3/19	25/1/19	Synchronizer failure and metastability	TB-2	ELX 404.2	PO1, PO3	
	Module:4 Introduction to VHDL							
	18	28/1/19	29/1/19	Introduction to hardware description language	TB-3	ELX 404.3	PO1,PO3,PO5	
	19	29/1/19	29/1/19	VHDL data types, concurrent and sequential statements	TB-3	ELX 404.3	PO1,PO3,PO5	
	20	7/2/19	7/2/19	Data flow, behavioral models	TB-3	ELX 404.3	PO1,PO3,PO5	
	21	8/2/19	7/2/19	VHDL codes for various digital circuits	TB-3	ELX 404.3	PO1,PO3,PO5	
	22	11/2/19	8/2/19	VHDL codes for various digital circuits	TB-3	ELX 404.3	PO1,PO3,PO5	
	Module: 2 Algorithmic state machine(ASM) chart and Register Transfer Language (RTL)							
	23	5/3/19	5/3/19	Standard symbols for ASM chart	TB-2	ELX 404.1	PO1	
	24	7/3/19	5/3/19	Realization techniques for sequential / logic functions using ASM chart	TB-2	ELX 404.1	PO1	
	25	8/3/19	7/3/19	ASM chart representation of control unit	TB-2	ELX 404.1	PO1, PO3	
	26	11/3/19	8/3/19	Waveform controllable generator, pulse width adjustor using ASM chart	TB-2	ELX 404.1	PO1, PO3	
	27	12/3/19	11/3/19	RTL construction of data unit using RTL description,	TB-2	ELX 404.1	PO1, PO3	

				Timing of connection and transfer				
	28	14/3/19	12/3/19	Combinational logic and conditional transfer	TB-2	ELX 404.1	PO1, PO3	
	29	15/3/19	12/3/19	Graphical and RTL bus notation , Design data unit using RTL description	TB-2	ELX 404.1	PO1. PO3	
	30	18/3/19	14/3/19	Design control unit using RTL		ELX 404.1	PO1, PO3	
		Module:5 Design of sequential circuits using VHDL						
	31	12/2/19	8/2/19	VHDL code for Flip flop, counters, registers	TB-3	ELX 404.3	PO1, PO5	
	32	18/2/19	18/2/19	VHDL code for Flip flop, counters, registers	TB-3	ELX 404.3	PO1, PO5	
	33	19/2/19		VHDL code for Moore type FSM	TB-3	ELX 404.3	PO1, PO5	Holi Holiday
	34	21/2/19	21/2/19	VHDL code for Mealy type FSM	TB-3	ELX 404.3	PO1, PO5	
	35	22/2/19	22/2/19	VHDL code for sequence detectors	TB-3	ELX 404.3	PO1, PO5	
	Module: 6 Programmable Logic Devices							
	36	25/2/19	25/2/19	Study of ROM, RAM ,SRAM using PLDs	TB-2,4 Rf-2	ELX 404.4	PO1	
	37	26/2/19	26/2/19	Design of various digital circuits using PLA	TB-2,4 RF-2	ELX 404.4	PO1, PO3	
	38	28/2/19	28/2/19	Design of various digital circuits using PAL	TB-2,4 RF-2	ELX 404.4	PO1, PO3	

	39	1/3/19	1/3/19	Study of CPLD and FPGA architecture		ELX 404.4	PO1	
		27/3/19	27/3/19	ASM Chart Problems		ELX 404.1	PO1	
		28/3/19	28/3/19	ASM Chart Problems		ELX 404.1	PO1	
		29/9/19	29/9/19	VHDL codes for various digital circuits		ELX 404.3	PO1, PO5	
	40	1/4/19	1/4/19	VHDL codes for various digital circuits		ELX 404.3	PO1, PO5	
			2/4/19	University question papers				
			3/4/19	University question papers				

Text Books:

1. Digital Logic Applications and Design – John M. Yarbrough, Thomson Publications, 2006
2. Digital Design, Morris Mano Second Edition, PHI, 2002
3. Volnei A. Pedroni, “Circuit Design with VHDL” MIT Press (2004)

Reference Books:

1. Digital Design Principles and Practices, 3rd ed. by Wakerly. Prentice Hall, 2000
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI
4. William I.Flectcher, “An Engineering Approach to Digital Design”, PrenticeHall of India.
5. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
6. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.
7. Stephen Brown, Zvonko Vranesic, “Fundamentals of Digital Logic Design” McGraw Hill, 2nd edition Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered as final IA marks.

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. The students need to solve total 4 questions.
3. Question No. 1 will be compulsory and based on entire syllabus.
4. Remaining questions (Q2 to Q6) will be set from all modules.
5. Weightage of each module in question paper will be proportional to the number of respective lecture hours mentioned in the syllabus

Practical Session Plan

CLASS	SE Electronics, Semester IV
Academic Term	Jan – May 2019
Subject	**Digital System Design Laboratory** (**ELXL403)**

Evaluation System		***Hours***	***Marks***
	Practical and Oral Examination		25
	Term work	--	25
	Total	--	50

Time Table	***Day***	***Batch***	***Time***
	Monday	***C***	***1:30 pm-3:30 pm***
	Tuesday	***D***	***1:30 pm-3:30 pm***
	Wednesday	***A***	***2:30 pm-4:30am***
	Thursday	***B***	***2:30 pm-4:30am***

Title of Experiments

Sr. No.	***Title***	***Module***	***Attained Pos***
1	Implementation of MOD-N **Asynchronous** counter using IC **7493**	Sequential logic design	PO1,PO3

		practices	
2	Implementation of MOD-N Up-counters **Synchronous** using **74163**	Sequential logic design practices	PO1,PO3
3.	Implementation of MOD **Up/Down counter** (Synchronous) using **74169**	Sequential logic design practices	PO1,PO3
4	Design and implement **Sequence Detector** using flip flop	Sequential logic design	PO1,PO3
5	Implement the Generic Multiplexer using VHDL with all modeling style and simulate the same with **Xilinx ISE** tool and observe the output on Spartan -6 FPGA.	Introduction to VHDL	PO1,PO3,PO5
6	Design and implement 4 bit counter with VHDL and Simulate the same on **ModelSim**.	Design of sequential circuits using VHDL	PO1,PO3,PO5
7	Design and implement frequency divider 10KHz to 1Hz with VHDL and simulate the same on **ModelSim**.	Design of sequential circuits using VHDL	PO1,PO3,PO5
8	Design and Simulate the **Finite state machine** using VHDL	Design of sequential circuits using VHDL	PO1,PO3,PO5
Newly added Experiments			
Implementation of MOD **Up/Down counter** (Synchronous) using **74169**		Sequential logic design practices	PO1,PO3
Design and implement 4 bit counter with VHDL and		Design of sequential	PO1,PO3,PO

Simulate the same on **ModelSim**.	circuits using VHDL	5
Design and implement frequency divider 10KHz to 1Hz with VHDL and simulate the same on **ModelSim**.	Design of sequential circuits using VHDL	PO1,PO3,PO5

Overall (all experiments together) mapping with Pos

	Programme Outcomes
HI(3)	***PO1,PO3***
MI(2)	***PO2,PO5***
LI(1)	***PO8,PO9,PO10,PO12***

Practical Session Plan

Experiment No. 1	Implementation of MOD-N **Asynchronous** counter using IC **7493**

Batch	***Dates***		***Remarks***
	Planned	***Actual***	
A	***16/1/19***	***16/1/19***	
B	***17/1/19***	***17/1/19***	
C	***14/1/19***	***14/1/19***	
D	***15/1/19***	***15/1/19***	

Experiment No. 2	Implementation of MOD-N Up-counters **Synchronous** using **74163**

Batch	***Dates***		***Remarks***
	Planned	***Actual***	

A	***23/1/19***	***23/1/19***	
B	***24/1/19***	***24/1/19***	
C	***21/1/19***	***21/1/19***	
D	***22/1/19***	***22/1/19***	

Experiment No. 3	Implementation of MOD **Up/Down counter** (Synchronous) using **74169**

Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***30/1/19***	***30/1/19***	
B	***07/2/19***	***07/2/19***	
C	***28/1/18***	***28/1/18***	
D	***29/1/19***	***29/1/19***	

Experiment No. 4	Design and implement **Sequence Detector** using flip flop/ Project Idea and its approval

Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***20/2/19***	***20/2/19***	
B	***21/2/19***	***21/2/19***	
C	***11/2/19***	***11/2/19***	
D	***12/2/19***	***12/2/19***	

Experiment No. 5	Implement the Generic Multiplexer using VHDL with all modeling style and simulate the same with **Xilinx ISE** tool and observe the

	output on Spartan -6 FPGA.		
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***27/2/19***	***27/2/19***	
B	***28/2/19***	***28/2/19***	
C	***18/2/19***	***18/2/19***	
D	***26/2/19***	***26/2/19***	
Experiment No. 6	Design and implement 4 bit counter with VHDL and Simulate the same on **ModelSim**.		
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***6/3/19***	***6/3/19***	
B	***7/3/19***	***7/3/19***	
C	***25/2/19***	***25/2/19***	
D	***5/3/19***	***5/3/19***	
Experiment No.7	Design and implement frequency divider 10KHz to 1Hz with VHDL and simulate the same on **ModelSim**.		
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***13/3/19***	***13/3/19***	
B	***14/3/19***	***14/3/19***	
C	***11/3/19***	***11/3/19***	

D	***12/3/19***	***12/3/19***	
Experiment No.8		Design and Simulate the **Finite state machine** using VHDL	
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***20/3/19***	***20/3/19***	
B	***28/3/19***	***28/3/19***	
C	***18/3/19***	***18/3/19***	
D	***19/3/19***	***19/3/19***	
Mini Project	Debugging the code		
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***27/3/19***	***27/3/19***	
B	***28/3/19***	***28/3/19***	
C	***25/3/19***	***25/3/19***	
D	***26/3/19***	***26/3/19***	
Mini Project	. Project Presentation		
Batch	***Dates***		***Remark***
	Planned	***Actual***	
A	***4/4/19***	***4/4/19***	
B	***4/4/19***	***4/4/19***	

C	***1/4/19***	***1/4/19***	
D	***2/4/19***	***2/4/19***	

Term Work:

At least 6 experiments covering entire syllabus of ELX 404 (Digital System Design) should be set to have well predefined inference and conclusion. The experiments should be student centric and attempt should be made to make experiments more meaningful, interesting. Simulation experiments are also encouraged. Experiment must be graded from time to time. Also each student (in group of 3/4) has to perform a ***Mini Project*** as a part of the laboratory and report of mini project should present in laboratory journal. The grades should be converted into marks as per the Credit and Grading System manual and should be added and averaged. The grading and term work assessment should be done based on this scheme. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. Practical and Oral exam will be based on the entire syllabus. Equal weightage should be given to laboratory experiments and project while assigning term work marks.