Dr.Swapnali Ashish Makdey

E: swapnalimakdey@gmail.com

M: +91 9769091874

Brief Overview:

- **Head of the Department of Electronics and Computer Science at Fr. Conceicao Rodrigues College of Engineering, Mumbai.**
- Completed a PhD in VLSI at the Centre of VLSI and Nanotechnology, Visvesvaraya National Institute of Technology, Nagpur.
- **Possess 25 years of experience in teaching and research.**
- Have a strong proficiency in **Digital VLSI, Analog VLSI Design, VHDL, Verilog System Verilog,**
- Experienced in managing projects related to Analog VLSI design, Digital VLSI Design, Verilog, and Machine Learning.
- **Familiar with EDA tools** like **Spice, EDA-Playground, Cadence-based tools such as Genus, Innovus, Virtuoso, etc**
- Strong presentation and communication skills to effectively deliver training sessions.
- Experience with both classroom and online training environments.
- Familiarity with e-learning authoring tools
- Demonstrated a track record of successful project development and implementations, showcasing strong technical, logical, analytical, and problem-solving skills.
- Possessing excellent interpersonal abilities and presentation skills, with the ability to quickly and comfortably connect with individuals from various cultures, personalities, ages, and business levels, and adapt rapidly to new geographies.

- **For the last 15 years, I have been responsible for setting examination papers for Analog VLSI Design (B.E Electronics) and Mixed VLSI Design (M.E. Electronics)** at Mumbai University

Certification: -

1. Completed the online training program on **VLSI DIGITAL IC DESIGN LABORATORY PRIMER** conducted from December 07, 2020 to January 16, 2021 by Entuple Technologies
2. Completed the online training program on **VLSI ANALOG IC DESIGN LABORATORY PRIMER** conducted from December 18, 2020 to January 16, 2021 by Entuple Technologies
3. Six weeks of **Professional Traine/ Internship on Python with Machine learning** on 28th March -11th May 2024 by Labview Academy
4. One-week Training Program on **Deep Learning** by Edulake Solutions
5. **Verilog HDL: VLSI Hardware Design Comprehensive Masterclass** (Udemy)
6. **System Verilog** for Verification (Udemy)
7. ATAL FDP on **'Semiconductor Digital System Design and Verification'** scheduled from Monday 11th Dec to Saturday 16th Dec 2023 at Fr. Conceicao Rodrigues College of Engineering
8. Organised **ATAL FDP on Applied Machine learning for VLSI Design** from 4th December 2024 to 9th December 2024
9. **Verilog HDL Fundamentals for Digital Design and Verification (Udemy)**
10. **VSD - Physical Design Flow (Udemy)**
11. One week on the Faculty programme on **"VLSI Design Using Cadence Tools:Mixed Signal VLSI Design"**
12. Participated in the one-day short-term training programme on**"Semiconductor Device Modeling using Visual TCAD & GENIUS 3D", organized by SPIT, Mumbai**
13. Participated in the one week short term training programme on **"Semiconductor Technology & Manufacturing" organized by CEP IIT Bombay**

Technical Skills:

- Thorough knowledge of **Analog VLSI Design and Digital VLSI Design, Verilog, System Verilog**
- Understanding of electronic devices, Microprocessors, Microcontrollers, and **Embedded Systems**
- Proficiency in Digital Electronics, Analog Circuits, Computer Networks, and Computer Organization
- **Exposure to complete RTL to GDSII flow.**
- **Physical design implementation using EDA tools**

Management Skills: -

- I currently serve as the **AP/ED Chair of the IEEE Bombay Section** and have been actively engaged as the **IEEE-GOLD Chair and the WOMEN Chair of the same section**. Additionally, I have fulfilled the role of Educational Activity Chair within the IEEE Bombay Section.
- My efforts have been crucial in advancing the department and organizing academic activities. Currently serving as a member of the Academic Council.
- As the **Technical In charge of the College**, I have successfully organized various technical events, including **Hackathons and Project Competitions**.
- Furthermore, I have taken on the responsibility of **Placement Coordinator** for the Department.
- **Role in IEEE-CRCE (Fr. Conceicao Rodrigues College of Engineering) Growth**:
  Joined as branch counsellor in 2007 when IEEE-CRCE was marginally active.
  Transformed the branch, boosting membership from 30 to over 80 students.
- **Events and Activities:**
  Initiated quality events to enhance students' technical knowledge and application. Organized workshops on robotics, soldering, and lab equipment; seminars on embedded systems, technical paper writing, and cloud computing. Led competitions like technical debates, paper presentations, and quizzes.
- **Inter-Collegiate Events:**
  The branch's activities were elevated from intra-collegiate to inter-collegiate level. In 2009, the IEEE-Bombay section awarded IEEE-CRCE the right to host the K Shankar National Technical Paper Presentation. In 2010, we organized the **All-India Student Congress (AISC),** a national-level IEEE event with participants from across India.
- **Personal Dedication:**
  Invested significant personal time, staying back late to ensure successful event preparation and execution. Acted as a mentor, motivator, and guide for students..
- **Social Commitment**:
  Encouraged students to hold a computer literacy workshop at an orphanage, Bal Vidya Bhavan, fostering a sense of community service.
- **Accolades and Awards:**
  Elected Women Chair of IEEE Bombay Council in 2009. IEEE-CRCE won Best Website Design at the R10 level and placed fourth internationally, which was appreciated by everyone.
- **Leadership Qualities:**
  Acted as a liaison between the student council and college management, securing support for IEEE initiatives. Ensured that IEEE activities did not disrupt students' academic progress.
- **International Recognition:**
  Hosted an IEEE Standards Association-USA workshop on Cloud Computing in 2011, which brought international attention to IEEE-CRCE.

Achievements: -

- I was honoured with the **Most Influential Professor Award** at a star-studded ceremony held at Hotel Taj Lands' End, Mumbai, on 19th November 2025.
- The research paper 'Harmony Guard: A Multimodal Approach to Hate Speech Detection in Hindi Audio' has been awarded the **'Best Paper in Track' Prize** for the Data Science, AI, ML, and DL track. in the 7th International Conference on Ideas, Innovation and Impact in Science & Technology organized on the 11th and 12th of June 2024 by Smt.Kashibai Navale College of Engineering, Sinhagad Institute, Pune
- **Received second prize at DIPEX2018 for the project "Rpiscope**: an Effective Tool for Farmers "
- Mentored the project titled," Rpi-scope an effective tool for farmers demonstrated at regional finals of e-yantra idea competition (eYIC-2019)
- Recognized as the best IEEE branch counselor in the IEEE BOMBAY section
- The IEEE-CRCE website was awarded the Third prize at IEEE Region 10 &Fourth prize at the international level, during my tenure as IEEE Branch counselor
- Worked as a judge in MP-Proex 2009, National Level Project Exhibition, Paper Presentation, and Technical Quiz contest.
- Received consolation prize in 'ELECTRAMA' 99 held at Mumbai for "PC based Greenhouse automation

Educational Details

- Completed PhD from Visvesvaraya National Institute of Technology, Nagpur. VNIT, Nagpur
- M.E. in Electronics Engineering from Fr. CRCE, Mumbai.
- B.E. in Electronics Engineering from Shivaji University, Kolhapur
- Diploma in Electronics Engineering from B.T. E. Board Please mention the year

Professional Membership; -

IEEE, ISTE, FSAI, VLSI Society of India

Invited Talks & Professional Engagements: -

1. **Resource Person** for a session on *"***Machine Learning in VLSI Design***"* during the FDP on **"Cadence Tools: Virtuoso & Verilog Design Flow"**, organized by the Faculty & Staff Development Centre, K J Somaiya School of Engineering in collaboration with C2S, on **5 December 2025**, at K J Somaiya School of Engineering.

2. **Chief Guest** for the Annual School Exhibition at **Dr. S. Radhakrishnan International School, Malad**, on **12 December 2025**.

3. **Resource Person** for the One-Day State Level Online Workshop **on "Mission Semiconductor: Empowering Atmanirbhar Bharat***"*, jointly organized by Phulsing Naik Mahavidyalaya, Pusad, on 10 October 2025 (Online Mode).

4. **Resource Person** for a session on *"AI Tools for Research"* during the Online FDP on **"AI Driven Smart Teaching Strategy"**, organized by **Ashokrao Mane Polytechnic, Vathar Tarf Vadgaon**, on **21 August 2025**.

5. **Resource Person** for a session on *"AI Tools for Research"* in the One-Week Faculty Development Program on **"Systematic Way of Research Paper Writing & Funding"** (Approved by AICTE), organized by **Sharad Institute of Technology, Polytechnic**, on **9 August 2025** (Online Mode).

6. Resource Person for a Faculty Development Program at SVERI's College of Engineering, Pandharpur, on 23 December 2024, where she delivered an expert session on "**Fusion of Semiconductor Advancements and AI Paradigms**."

7. Participated in **SEMICON 2025 at Delhi and SEMIX at IIT Bombay**, where she interacted with industry leaders, researchers, and technology experts to explore advancements in semiconductor manufacturing, VLSI design, and strategic industry–academia collaboration.

Publications: -

In Journal

1. Ninad More, **Swapnali Makdey**, Puja Padiya, Kranti Vithal Ghag, Ankush Pawar, Nilesh Marathe, "Novel Applications of Deep Learning in Remote Sensing Satellite Imagery: Natural Hazards and Disasters Risk Management" Journal of Information Systems Engineering and Management, Vol. 10 No. 26s (2025),e-ISSN: 2468-4376 **Elsevier (Scopus indexed)**
2. **Dr. Swapnali Makdey**. Dr.Ashok Kanthe, Dr. Ninad More,"" A Novel Neural-Based Design of Graphene and Molybdenum Disulfide Magnetic Tunnel Junction", 2025, 10(11s)e-ISSN: 2468-4376 DOI: https://doi.org/10.52783/jisem.v10i11s.1668" **Elsevier (Scopus indexed)**
3. Dr.Ninad More, **Dr.Swapnali Makdey**, Kirti Wanjale, Puja Padiya, Nilesh Marathe, Kranti Vithal Ghag,"A New Approach to Natural Language Query Search using Frequency Analysis Techniques in Cloud Computing "Journal of Information Systems Engineering and Management, 2025, 10(11s)e-ISSN: 2468-4376 DOI: https://doi.org/10.52783/jisem.v10i11s.1669" **Elsevier (Scopus indexed)**
4. "Nilesh P. Sable, Kirti H. Wanjale, **Dr. Swapnali Makdey**, Ketan J. Raut, Ashok Kanthe, Varsha Jadhav, "Efficient Component Packing with Algorithmic Optimizations" "Journal of Information Systems Engineering and Management,2025, 10(9s),e-ISSN: 2468-4376,DOI: https://doi.org/10.52783/jisem.v10i9s.1240. **Elsevier (Scopus indexed)**
5. **Makdey, Swapnali**, Rajendra Patrikar, "Modeling and implementation of spin diode based on two-dimensional materials using Monte Carlo sampling method." Circuit World 47, no. 4 (2020): 357-367.(**SCI**)
6. **Makdey, Swapnali Ashish**, and Rajendra Patrikar. "Design of behavior prediction model of molybdenum disulfide magnetic tunnel junctions using deep networks." Semiconductor Science and Technology (2023). (**SCI)**
7. Narwade, Sharda P., Anish U. Bhurke, and **Swapnali Makdey**. "Study on Performance of 22nm Single Gate and Multi-Gate MOSFET." *International Journal of Scientific Engineering Research-IJSER15982* 4, no. 10 (2016).

8. Surwadkar, Tushar, **Swapnali Makdey**, Deepak Bhoir, and D. Bhoir. "Upgrading the performance of VLSI circuits using FinFETs." *International Journal of Engineering Trends and Technology* 14, no. 4 (2014): 179-184.(**Scopus indexed)**
9. Dattaprasad Madur , Dr. Deepak Bhoir, .**Swapnali Makdey,"**Three Dimensional integration of CMOS" International Journal of Electronics and Communication Engineering and Technology (IJECET 2014-15), Volume 5, Issue 11, November (2014), pp. 01-05

In Conference

1 Mohit Pansare, Pratham Mahajan, Sakshee Patil and Prof. Swapnali Makdey , "A Multimodal Approach to Hate Speech Detection in Hindi Audio" 7th International Conference on Ideas, Innovation and Impact in Science & Technology,11-12June 2024,(**awarded the 'Best Paper in Track' Prize for the Data Science, AI, ML and DL track)**

2 **Makdey, Swapnali**, Rajendra Patrikar, titled," 2D Material Based Varactors" in the 5th International Conference on Nanoscience and Nanotechnology (ICONN-2019) to be held at SRM IST during Jan 28-30, 2019.

3 **Makdey, Swapnali**, Rajendra Patrikar," Effect of the 2D material-based insulator in Magnetic tunnel junction" "12th World in Congress on Graphene Technology & Materials Chemistry" at Kyoto, Japan for November 25-26, 2019.

4 Akhil Ulhas Masurkar, **Swapnali Mahadik** "Optimization of Subthreshold Slope In Submicron MOSFET's For Switching Applications," Advances in Computing, Communication, and Control,Spinger, ICAC32013, CCIS361,PP712-720,2013

5 Akhil Ulhas Masurkar, **Swapnali Mahadik** "Optimization Of Subthreshold Slope In Submicron MOSFET's For Switching Applications," Advances in Computing, Communication, and Control Spinger, ICAC3 2013, CCIS361,PP712-720,2013**(Scopus)**

6 Akhil Ulhas Masurkar**, Swapnali Mahadik** "Optimization Of Subthreshold Slope In Submicron MOSFET's for Switching Applications," INDICON 2012, pp1200-1204**(Scopus)**

7 Akhil masurkar Swapnali mahadik " Optimized Estimation of Drain to source currents in submicron MOSFETs using MATLAB|" in the procedding of ISCI 2012

8 Akhil masurkar,Swapnali Mahadik " Mitigating Techniques to reduce Sub-threshold currents in submicron MOSFETs" in the procedding of "International Journal of scientific & engineering Research volume 3 issue 5 May 2011

9 Swapnali mahadik , Prof. D. V. Bhoir, K Narayanan " Access control System using fingerprint Recognition" in ACM Digital library, Proceedings of the International Conference on Advances in Computing, Communication and Control,ICAC3'09, 2009, pp. 306–311 (**Scopus)**

10 Shah, D., Mahadik, S, "QoS oriented failure rate-cost and time algorithm for compute grid" Proceedings of the International Conference on Advances in Computing, Communication and Control,ICAC3'09, 2009, pp. 264–267 (**Scopus)**

ATAL/UGC/AICTE FDP:-

1 Ten Days Online Winter Faculty Development Program on “Intricacies of Analog & Mixed Signal IC Design” jointly organized by Electronics & ICT Academies held from 17th – 26th February, 2025 through National Knowledge Network under the “Scheme of Financial assistance for setting up of Electronics & ICT Academies” by the Ministry of Electronics and information Technology (MeitY), Government of India. This Programme is endorsed by AICTE/UGC/NBA.

2 AICTE Training And Learning (ATAL) Academy Faculty Development Program on Artificial Intelligence Techniques in VLSI Design at PSNA College Of Engineering And Technology, Dindigul from 20/01/2025 to 25/01/2025.

3 AICTE Training And Learning (ATAL) Academy Faculty Development Program on Navigating the Future of Decentralized Advanced Blockchain Technologies at Fr. Conceicao Rodrigues College Of Engineering from 09/12/2024 to 21/12/2024.

4 ATAL FDP on 'Semiconductor Digital System Design and Verification' scheduled from Monday 11th Dec to Saturday 16th Dec 2023 at Fr.Conceicao Rodrigues College of Engineering

5 AICTE Training And Learning (ATAL) Academy Online Elementary FDP on "Machine Learning Applications in Micro-Nano VLSI Technologies" from 21/06/2021 to 25/06/2021 at BVRIT HYDERABAD College of Engineering for Women .

6 One Week Online Short Term Training Program on “VLSI Design Using Cadence Tools: Analog CMOS VLSI Design" sponsored by AICTE, New Delhi (Ref: F.No. 34-65/345/RIFD/STTP/Policy-1/2018-19 dated 10/01/2020) during 2 nd Nov 2020 to 7th Nov 2020 organised by SPIT Mumbai

7 One Week Online Short Term Training Program on “VLSI Design Using Cadence Tools: Mixed Signal VLSI Design" sponsored by AICTE, New Delhi (Ref: F.No. 34-65/345/RIFD/STTP/Policy-1/2018-19 dated 10/01/2020) during 30th Nov 2020 to 5 th Dec 2020 organised by SPIT Mumbai.

8 Successfully completed faculty development program on LaTeX organized at Sanjay Ghodawat University in association with theSpoken Tutorial Project, IIT Bombay from 27th April to 2nd May 2020

9 Participated in the two weeks short term training programme on Hands on Training on “Multiscale Simulation in Advanced Materials Science & Technology (HTMSAMST-2016)" during14-24 July 2016, SVNIT, Surat

Industrial Training / Professional Training: -

1. The Six weeks Professional Training/Internship Program on Python with Machine Learning from 28th March - 11th May 2024 under the Center of Excellence, National Instruments Innovation Center Greater Noida. Issued date is 23rd May 2024 with Reference No NIIC/COE/SI/ 0524-882.
2. The online training program on VLSI Analog Ic Design Laboratory Primer conducted from December 18, 2020 to January 16, 2021by Entuple Technologies
3. The online training program on VLSI Digital Ic Design Laboratory Primer conducted from December 07, 2020 to January 16, 2021 2021by Entuple Technologies

4. 5 Days on Data Science Workshop and Internship from 20th July 2020 to 24th July 2020 by Greyatom
5. One Week (10 hours) live Online Industrial Training on Deep Learning held on 18 - 22 March 2024 Organized by EduLakes Solutions LLP In Association with National Service Scheme (NSS) - IIT Roorkee.